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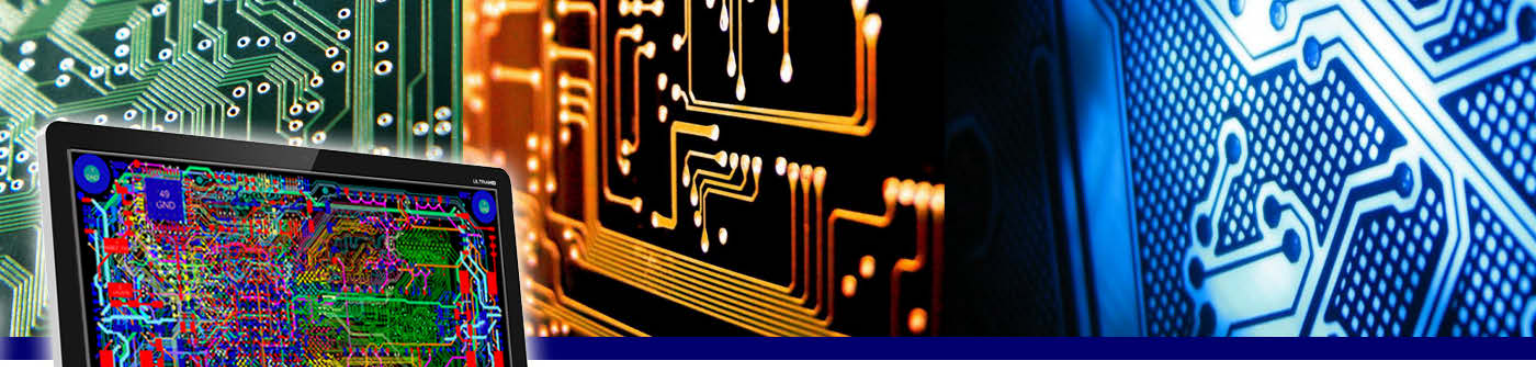

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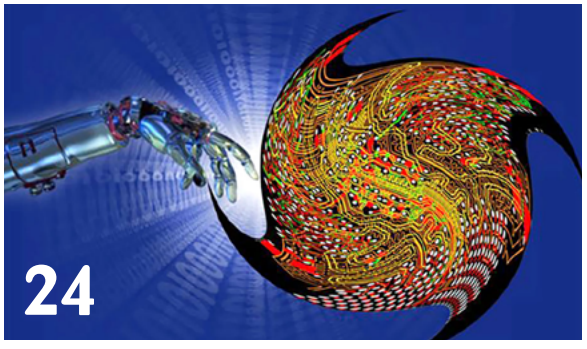

EDA Tools: Automation or Control?

PCB designers get downright exorcised about their EDA tools. One point of contention has to do with automation itself: How much is too much? Some designers prefer manual control—not just for routing, but for much of the layout. Others want as much automation and horsepower as they can get. This month, our feature story by Intercept Technology's Abby Monaco highlights the challenges EDA software companies face trying to give designers the power, and control, that they need. UTC's Stephen V. Chavez explains why he prefers a mix of control and automation, and why mastery of each EDA tool is critical. Guest Editor Kelly Dack discusses why he prefers manual control for autorouting and more. And Barry Olney explains why artificial intelligence should be built into EDA tools from scratch, citing some of the repetitive tasks that could be addressed easily with AI.

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Vol. 5, No. 5

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46

52

60

More Content

The Designer Roundtable Roundup

by Andy Shaughnessy
I-CONNECT007

Every year, I attend SMTA Atlanta, just across town. You have to love a local trade show! No airlines, no jet lag, and no hotels. It's a small show; it would fit in a school gymnasium.

Regional tabletop shows like this may be the next big thing. Fees for exhibiting are so low that it's hard to justify not exhibiting. Some companies had their local reps manning the booths, but I talked to exhibitors who flew in from all over the East Coast, including one technologist from Canada. If you can tie in a few customer visits, the trip can pay for itself.

But for me, the highpoint of SMTA Atlanta is the Designers Roundtable. This informal gathering usually draws about a dozen PCB designers, some of them ex-Scientific Atlanta veterans. It's moderated by UPMG's Pete Waddell, and we bounce questions off the designers for an hour or so. It's very informal, and it draws many of the PCB designers in metro Atlanta.

This year the roundtable had 15 attendees, up from 12 last year. Two of the new attendees were under 35, which surprised all of us. They design medical boards, which isn't such a surprise; that's one segment that keeps on growing. Most of the designers attending work for Cisco, Siemens, Sienna, NCR, and a few other smaller firms.

A few takeways: None of these designers thought much of solder mask-defined pads, because they create more problems than they solve.

• They don't trust CAD vendors' libraries, and there's not much love for OEMs' libraries either. One designer said he spends hours re-inventing the wheel designing footprints he's used before.

• They didn't see much hope for the new "pay per use" license being floated by companies like ANSYS. One designer said that soon they'd all be back renting mainframe time like it was 1987 all over again.

• As always, most designers at the roundtable have a love/hate relationship with their EDA tools. One Cadence user said he really loves his tool's horsepower, but he's glad Dal Tools makes Cadence tools work better.

• None of these attending designers, or even their companies, use signal integrity or EMC simulation. One designer said, "All of the simulation in the chip is already done."

• Most of these designers don't like updating their EDA tools because each new rev of the tool contains even more errors than the previous rev.

I told the crowd about Dale Parker's keynote at the IPC APEX EXPO Design Forum. I asked what they thought about Dale's assertion that the 1990s-era code for most EDA tools should be rewritten from scratch, with native artificial intelligence built in. Most of them thought AI had no place in EDA tools. One designer said, "But we're the artificial intelligence!"

I was glad to see more designers attending the roundtable this year, and even happier to see some designers without a drop of grey hair. We're seeing more and more "youngsters" all the time. Is this industry finally turning hip and cool?

Control vs. Automation

This month, we take on a subject that's come up in various surveys we've conducted over the past year: How much automation is too much in your design tool? How much manual control should a designer have? Some of you apparently turn everything off, and wish you could go back to hand-taping, while others want as much automation as you can get.

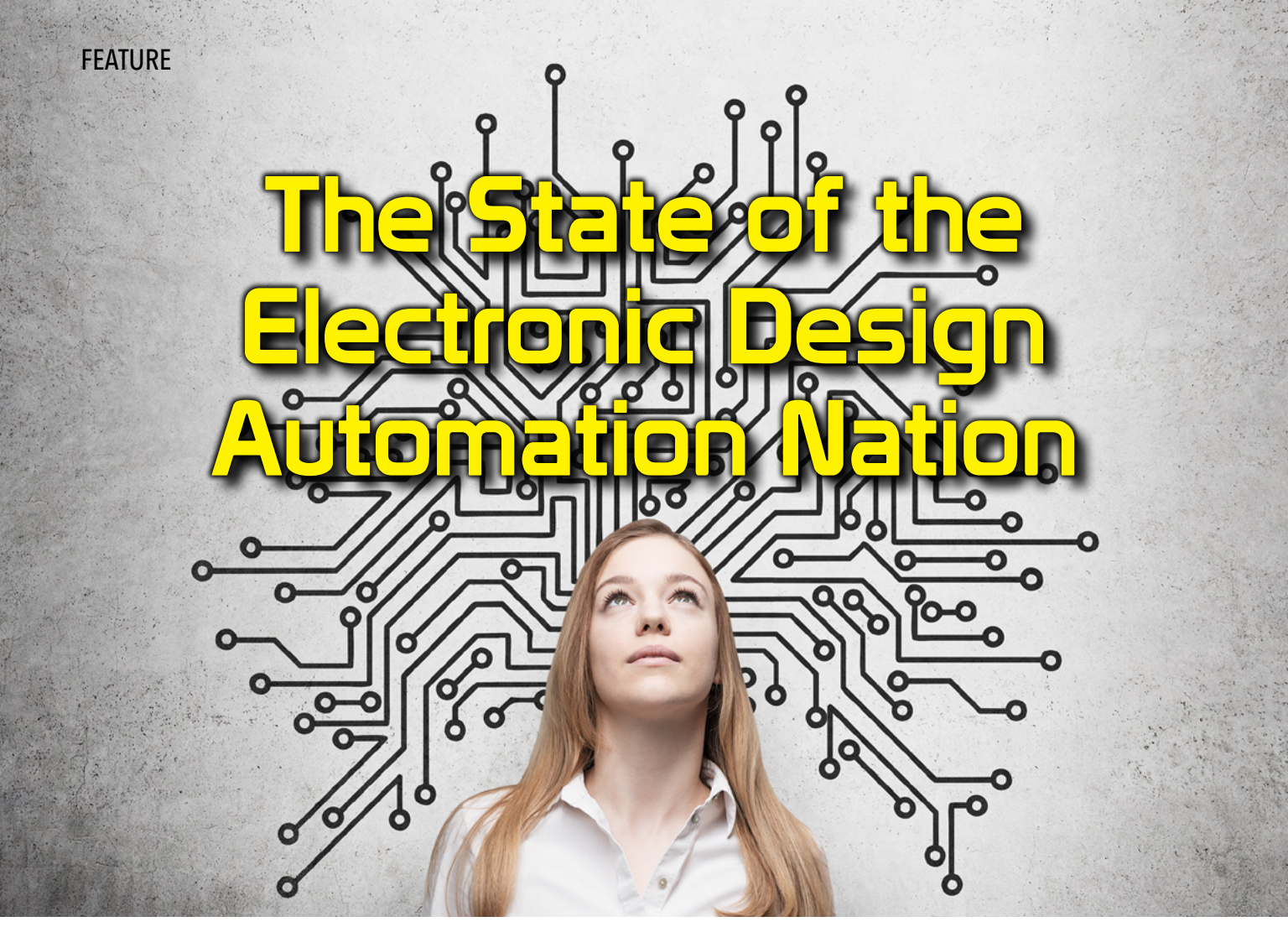
In our cover story, Abby Monaco of Intercept Technology discusses the changing landscape of PCB design tools, and lays out some of the steps Intercept has taken to provide more automation and greater control, along with the attendant trade-offs.

In an interview, UTC's Stephen V. Chavez, a frequent speaker at the Design Forum, explains why he prefers a combination of control and automation, and why mastery of your tool is paramount. Guest Editor Kelly Dack discusses, in an interview, why he prefers manual control for tasks such as autorouting, and why such preferences are usually based on a performance problem found in full automatic mode. And columnist Barry Olney explains why Dale Parker's push for AI in EDA tools is dead-on, starting with automating many of the repetitious tasks involved in every design.

What do you think about the idea of having artificial intelligence built into your EDA tools? Let me know what you think! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 16 years. He can be reached by clicking here.

The State of the Electronic Design Automation Nation



by Abby Monaco
INTERCEPT TECHNOLOGY

We are the automation nation. We are the high-speed demons, the low-frequency artists, the mixed-signal designers that make up the electronic design automation industry. We spend most of our working lives behind software, delivered to our fingertips with the promise of making things easier, faster, better, and getting us to our deadlines ever faster.

As a dedicated software product manager and a hands-on marketing director, I've seen trends in the efforts of software vendors to deliver automated portions of the design cycle. Some areas have been a great success, some areas have been a partial success, and some have just flopped all together.

There is an increase, year-over-year, in resources spent on the software vendors' side to help end-users reach success on a per project basis. There is a greater cry for freedom from designers who feel hampered by their very constrained, overly populated boards. Automation is a big part of the picture in these cases, and the growing complexity of PCB designs begs the question of where we begin to see diminishing returns on these efforts to make design "simpler" to accomplish. So often, a software tool promises a miraculous boost in productivity, only to leave users spending the same or more time correcting the automated processes that simply can't complete an area of design that needs fine tuning from an experienced hand.

Trends in the Beginning Phases of Design

The Automatic Stackup Builder

As PCB design software has matured, more and more of the processes outside the actual design have become incorporated into the design cycle. One such error-prone area is the PCB designs and the actual substrate onto which they will be manufactured. Basic CAD systems tend to only define the number of routing layers, which

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is a gross simplification. A typical FR-4 board is layer upon layer of core and prepreg materials that have specific heights and requirements. Even the typical copper route has a height that should be taken into account. As designs are becoming denser and more complex, greater attention is given to how to design a stackup with the best materials and configuration that satisfy both cost and the design requirements.

To aid designers and engineers in this area of greater attention, there is a movement toward pre-layout, software driven, stackup builders which help predict the board characteristics more accurately, and with greater signal integrity, which reduces the need for as many design changes throughout the layout process. Engineers and designers can more closely examine a board stackup, with visual cues for dielectric (prepreg) layers in between metal layers, blind and buried vias, as well as trace widths and heights within the stack. They can also attempt to prevent unexpected manufacturing flaws because many of these stackup builders include the manufacturer's specs or allow companies to build their own proven specs into the system for reliable re-use.

Since there are a vast number of manufacturers, and so many of them tend to have their own specs, Intercept chose many years ago to upgrade its stackup options to take height, dielectrics, and materials into account for easier output and drawing creation. But a more widely recognized expert in this area is Polar Instruments Inc., which has created its Speedstack tool set to allow quick and accurate stackups to be built and analyzed prior to the actual layout phase of the design cycle. They have even begun offering materials libraries that are either a generic set of information for easy building, or an actual list of materials as specified directly from some manufacturers. *(Note: Materials libraries are offered as a service to customers, but are not guaranteed to be fully up to date at any given time.)*

The Constraint Browser

Nearly every mid-to-high-end software vendor now offers full design constraint capabilities, from building simple design rules all the way to complex, formula-driven high-speed constraints. This is an area of automation that has allowed a boom in the high-density board

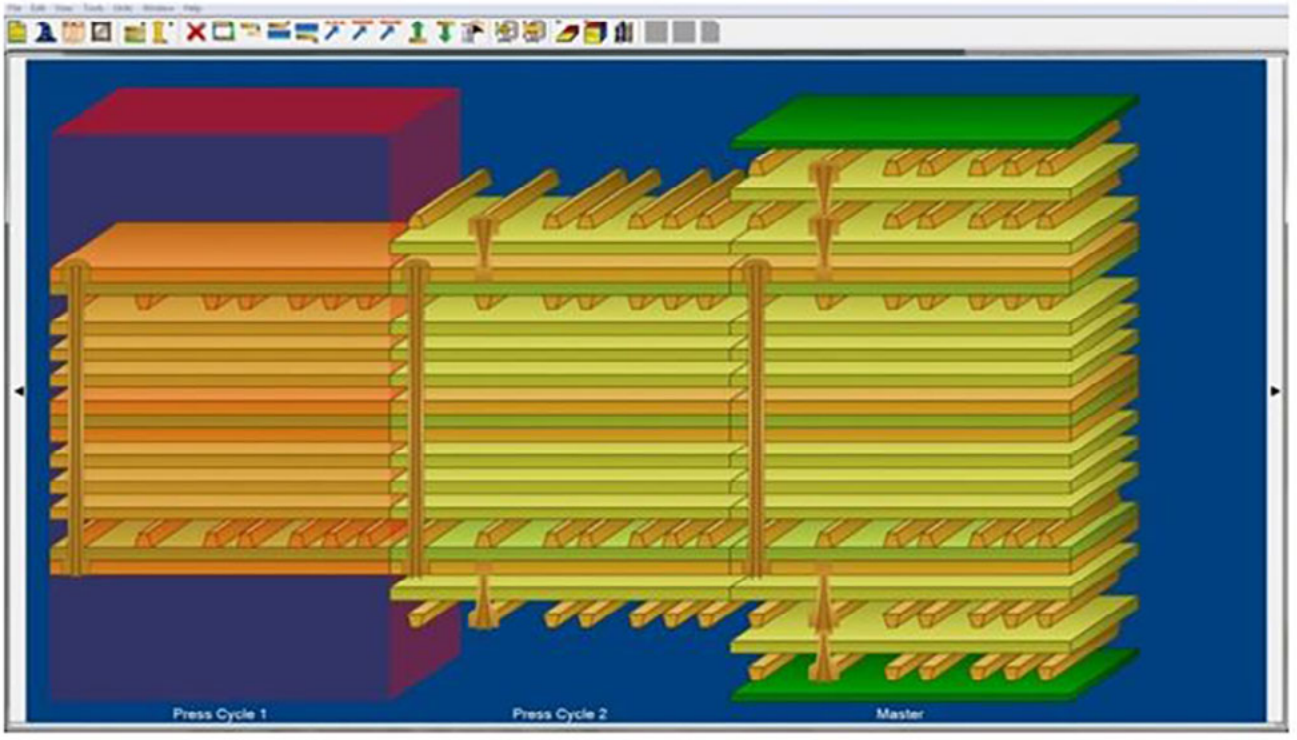

Figure 1: A view of a stackup built in Polar Instruments' Speedstack HDI software.

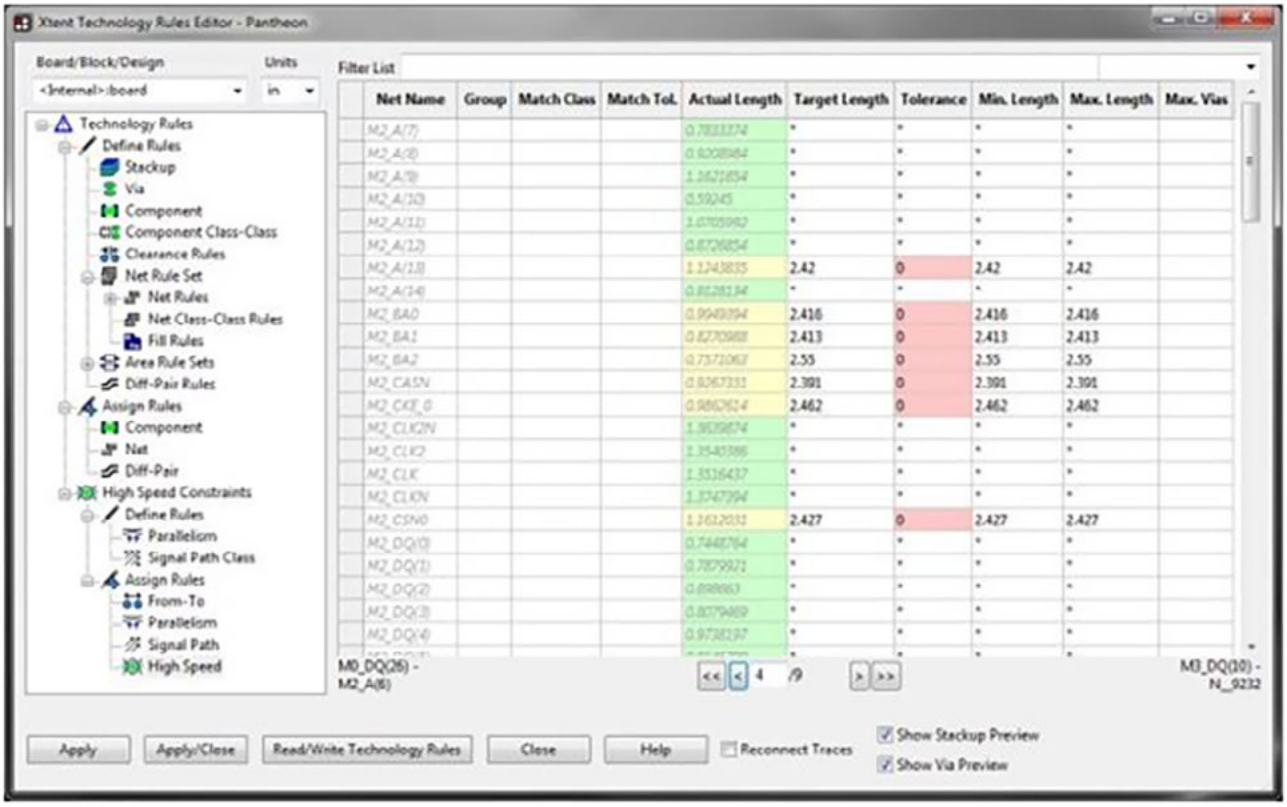

Figure 2: Intercept's constraint browser.

design area, has made autorouting ever more powerful, and has eased the headaches of high speed design requirements.

But this area of automation is a nightmare for some, while others sometimes find that the functions they really need simply aren't available. Some EDA software programs aimed themselves squarely at the electrical engineers with more of a chip design mindset, which ended in programs offering a confusing maze of endless possibilities, to the point that no one could achieve any productivity gains. Some call this the familiar "giving them the whole kitchen sink" approach, which software programmers familiar with the importance of the user experience would call an epic fail. It doesn't matter how brilliant your engineer is, the days of keeping a manual beside your digitizer and cards sitting over your function key options are over.

Intercept's approach to this movement was to build a constraint browser that offers a high level of functionality, just under the surface of a much simpler-to-use set of options. Constraining a board has to be done in a systematic, simple fashion, or it will become over constrained, unroutable, and time-consuming to complete. With Intercept's constraint browser in its Mozaix schematic and Pantheon layout software, users are presented with sets of options that layer upon one another. Simple net clearance rules are set up first, and then area rules can be defined where specific areas of the board don't fit the main clearance rules. This can be made more intricate if needed by adding class-to-class rules, or via or component rules. For designs with diff pairs, there are options to define diff pair rules and net constraints.

Finally, there is a full section in Intercept's constraint browser dedicated to just high speed constraints. This is the area where there seemed to be a desperate need to simplify what designers and engineers are trying to accomplish. To make it easier for users, the Intercept constraint browser presents itself very simply as a way to select net names and constrain them to specific minimum and maximum lengths. This seems to be what most high speed designers are happy to use as-is. But behind this surface are many

more options, such as adding equations into cells instead of hard values, or even creating signal paths to chain a full set of nets together from the beginning of the signal all the way to the end. The levels of complication can become great, but with Intercept's interactive checking throughout the browser, users are steered away from creating impossible configurations.

It is imperative to note here that while the automation of design constraints is now readily available in most EDA software, it still remains incumbent on the users to understand what they are doing. While some software vendors might present things in easier or harder to accomplish ways, it is still ultimately the engineer or designer who will help or hurt the design process.

Trends in the Middle Phases of Design

Auto-Placement

The concept of laying out the components on a board automatically is not new, but it is a constant area of development. Placing components by functional region, placing them per defined groups, or using assisted placement from the schematic has been around in some form or fashion. It is fair to say that most vendors offer some or all of these features to make placing components faster and easier, and that they tend to do the job of saving time well enough.

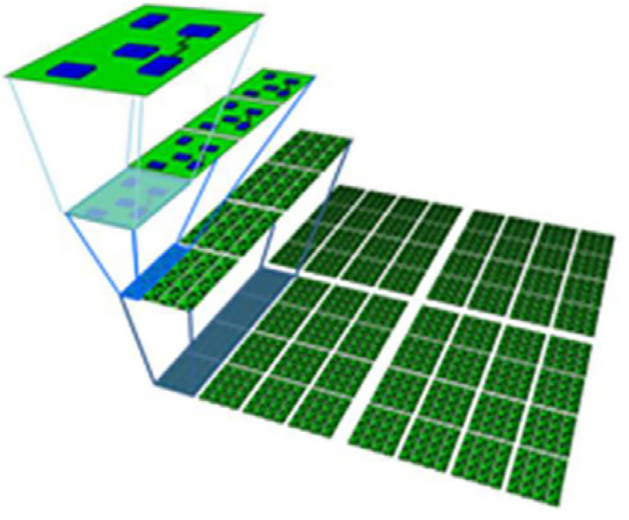

Figure 3: Example of design reuse as applied to a panel array design.

But beyond single component placement, EDA software vendors have moved into the area of blocks of functional components and their circuitry. These circuits are placed in a library for reuse and revision tracking, and are pulled into a layout for placement any number of times. Many vendors handle the reuse of blocks of circuits through a glorified copy-and-paste mechanism, which often presents problems because the copies are not traced back to their original, or they are not checked as part of the whole physical board.

Intercept's strategy was to develop a fully intelligent and reusable block of circuitry in Pantheon, called a "block geometry." Areas of circuitry that are used over and over again with little modification can be defined as block geometries and placed into the layout as a block array in a matter of seconds, and modified where needed without losing its links back to its parent block geometry. This allows major revisions of the block to be updated across the entire layout, with individual modifications (such as moving a component to avoid a drill hole) preserved. Repetitive circuits can even be defined as blocks within blocks, thus allowing design changes to be done in a matter of minutes. This technology has been used by Intercept's customers to place entire block panel arrays in minutes, whereas in the past it might have taken days.

Autorouting

Autorouting has been around for a very long time. But the trends surrounding it are changing. The simplest autorouters use a mixture of net class spacing and width constraints along with a layer's specified autoroute directions (horizontal/vertical, axial/diagonal, etc.), and attempt to generate successful pin-to-pin routes. These autorouters tend to create some nasty routes that are nowhere close to the desired result. But it is generally accepted that while these routers require further work to fix some of the anomalies that occur along the way, they are still saving time in the end.

But for the growing number of high density boards, or boards with diff pairs and high speed tuning, there is a movement toward throwing

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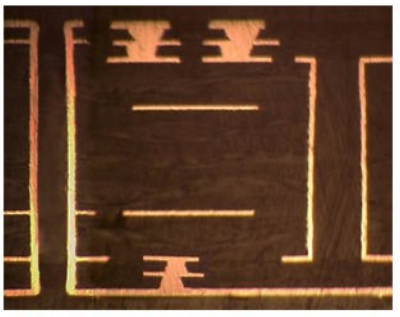

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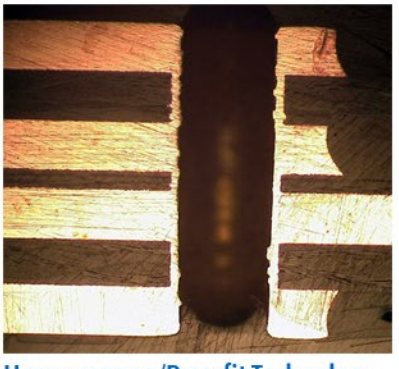

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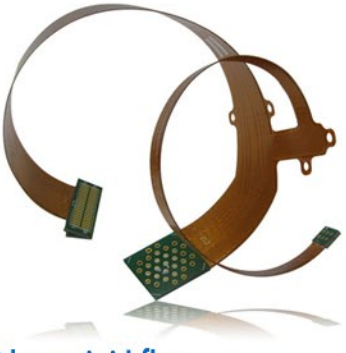

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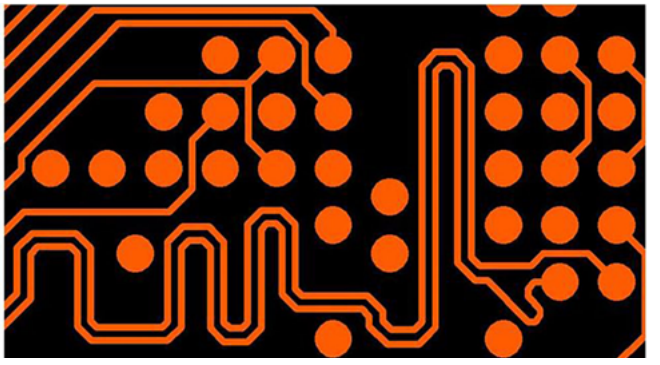

Figure 4: As higher densities, tuning and diff pairs become more prevalent in mainstream PCB designs, autorouters are struggling to keep up with more complex anomalies. It becomes a question of whether such anomalies are worth trying to algorithmically improve, or whether hand routing is returning to the picture.

out the autorouter all together. Designers have begun realizing that spending all their time trying to get a good outcome in a complex autorouting environment is an equivalent or even longer phase of the design cycle than if they simply hand routed sections of their board.

The reason for this is because autorouters require certain setup for a good outcome. Mainstream designs are becoming full of BGA breakouts, diff-pairs and nets tuned in all axes (not just X and Y, but through the Z as well!), and areas where all these complexities neck down and tune under completely different rules. But teaching the autorouter all of this can sometimes take so long that the user might as well have used manual routing to accomplish what in many cases is a better outcome than anything a routing algorithm could produce.

To better fill in for the gaps in the full autorouters, EDA vendors are now offering some very nice semi-automatic routing options such as routing all wires of a bus line together, routing and tuning diff-pairs one at a time, or region at a time, and handling breakouts from dense pin arrangements in various systematic ways. The very basics of the process are also improving with better visualization such as real-time, guided routing and quick via placement without the need for so many mouse clicks. All of these options are continually honed and improved, providing greater flexibility in response to designers' increasing level of difficulty.

While EDA software has run the gauntlet between fully manual, to fully automatic, to everything in between, it's fair to say that auto-routing will remain an ever-evolving area of the design cycle. The vendors all provide tools to help users get their jobs done, with different strengths and weaknesses, but it seems that the sweet spot for this area of design is in the semi-automatic: neither manual, nor fully automatic.

Auto-Tuning

High-speed design and auto-tuning are an area of complexity that are continually running into roadblocks. There is no advisable fully automated solution to this area of design. Try auto-tuning 24 wires all at once, and you have no-win collisions. Try just a few wires at a time, and your remaining wires can't find enough space to trombone their way together. Back and forth you go, until you delete all the wires and start manually tying up wire after wire, using every mil of space you can to save space for the next tune.

But here is the ingenuity of it: as you are stuck routing your wire and tuning as you want it tuned, automation is right at your fingertips.

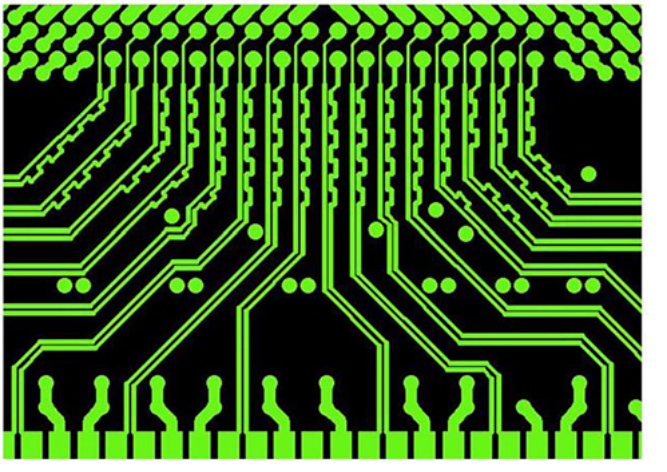

Figure 5: Programming a full autorouter to break out a diff pair bus line and tune the pairs accurately could take hours. Using newer bus line routing options and auto-tuning per diff pair to allow for close checking of the outcome has become much preferred among designers.

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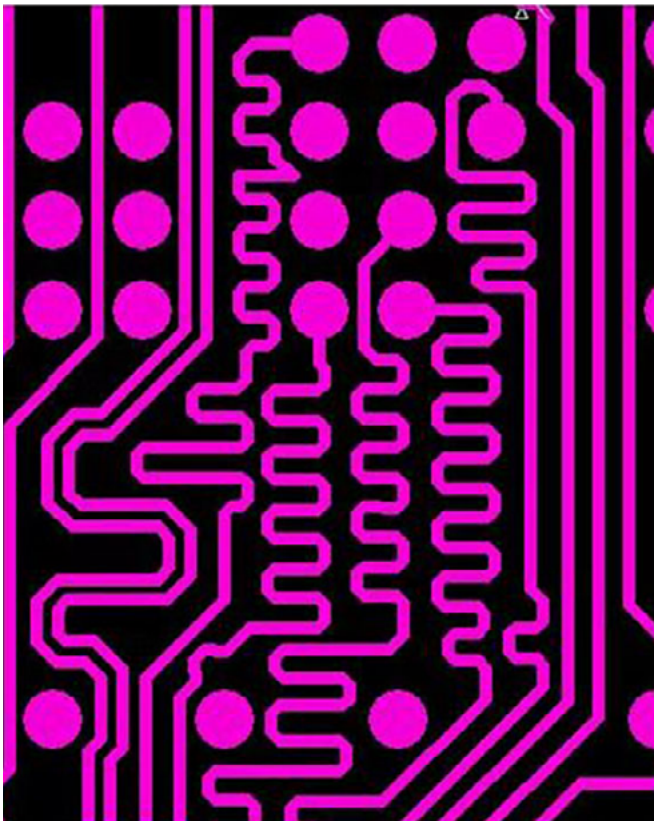

Figure 6: Tuning in tight areas can be a nightmare, whether automatic or manual.

With Intercept's Pantheon, the wire displays in red if you make it too long, blue if make it too short, and the target length is continually reported at the cursor tip so you know how you are doing along the way. Here we are, again concluding that sometimes only the semiautomatic method can be the real winner in the end.

Trends in the Completion and Post-Processing Phases of Design

Bill of Materials Creation

It seems that no matter how many flexible options software vendors offer, bill of materials creation remains a largely customized, scripted affair across a large portion of the industry. Every manufacturer has different BOM requirements and formatting expectations, and every EDA customer uses slightly different methods to specify the same information as everyone else. The result is that no matter how flexible the EDA software vendor tries to make the process of BOM creation, it seems to fall short in one way or another.

Intercept attempted to address these issues in both its Mozaix schematic and Pantheon layout applications by collecting information from every customer with a custom BOM output process and collating each requirement into common needs and special needs per customer. Common needs were addressed first, such as column width definitions, which property values to output, adding custom company headers, template setup, and real-time preview of the BOM output to aid the setup process. Then, to address the various needs of customers beyond the basics, two separate generic report tabs allow for customized reports to be appended to the BOM report, or output as separate files.

But on and above these efforts, it seems that greater unification of file formats among manufacturers is needed to really smooth this process into something that can be automated. With so many manufacturers across the country, this is probably not a likely change in the near future, and this output will probably continue to lack an easy path toward automation.

FAB & Assembly Drawings

It is fair to say that many EDA vendors have earned a bad reputation in the area of fabrication and assembly drawing output capability. For all the sophistication offered to accomplish the PCB layout, it is often a nightmare getting the finished layout submitted for fabrication. Some vendors use DXF outputs to AutoCAD or third party processing applications to aid the assembly and fab drawing process, which is an embarrassing admission of failure for the EDA software vendors. This is also a breakdown in the design cycle and can introduce errors between the finished board and the actual drawings that get sent for fabrication.

One such company that has helped the industry quite a bit in this area is Downstream Technologies. Their flagship product, BluePrint PCB, offers easy to use software to aid designers with the final post-processing phase of the design cycle. They have done a very nice job of addressing areas where EDA vendors have fallen short.

But not all vendors are completely without drawing capabilities. For the applications that

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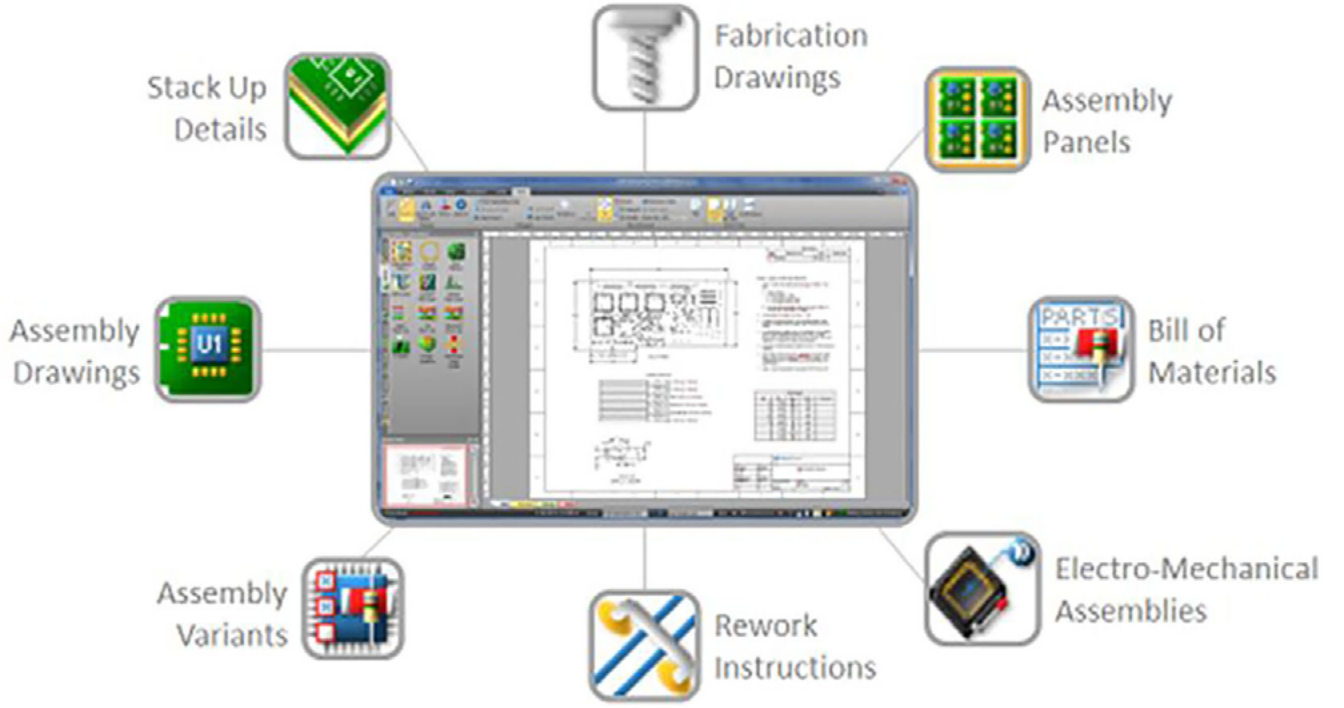


Figure 7: BluePrint-PCB helps designers produce comprehensive electronic drawings to drive PCB fabrication, assembly and inspection processes.

try a little harder, the job can be more manageable but is still time consuming. For example, many require designers to continually edit and output the same drawing time and again because there is no way to view the board more than one way on a drawing. This means that the finished drawing document may or may not be able to be produced again when back in the layout software.

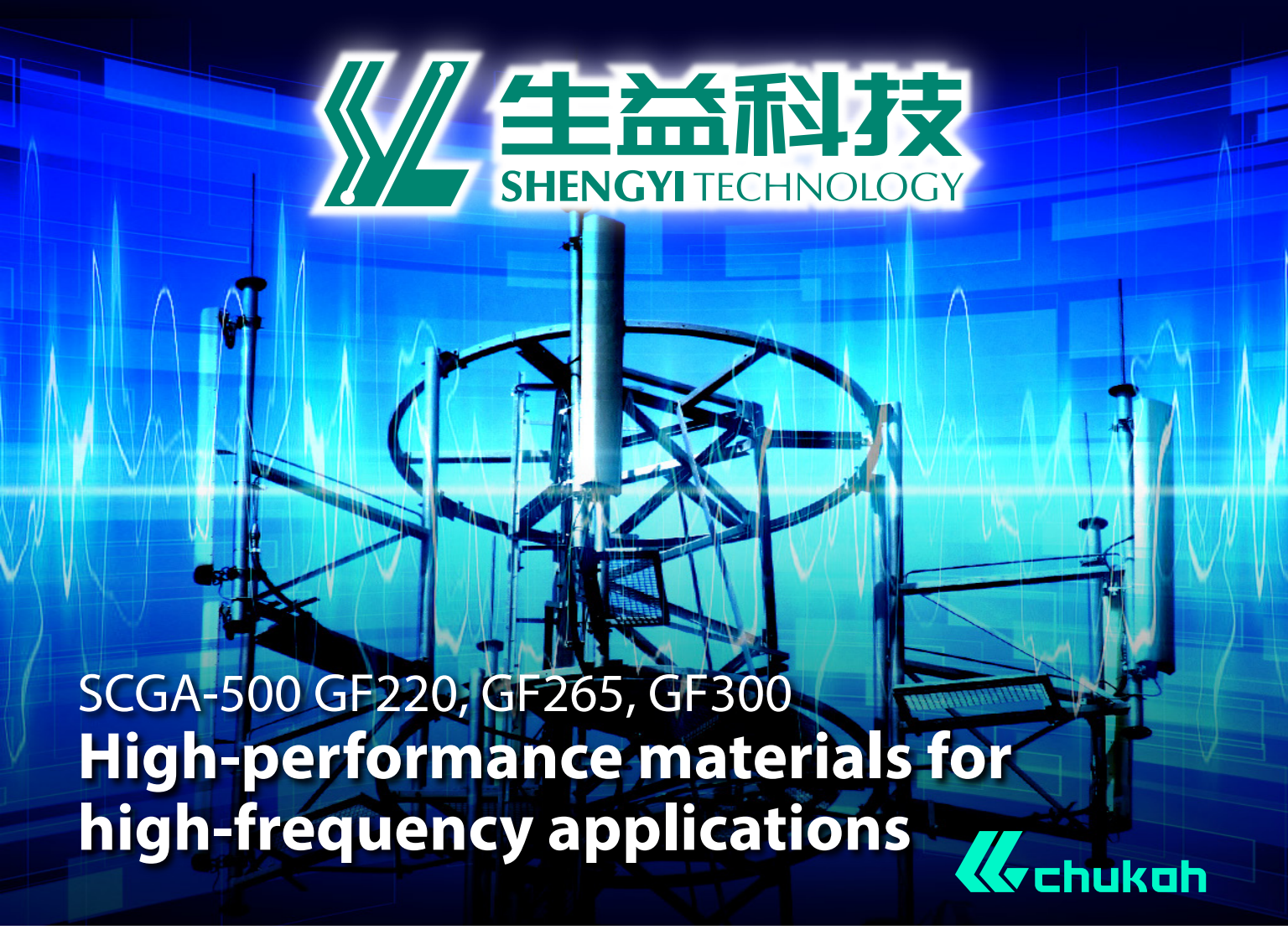
This is an area where Intercept has remained fairly strong. Drawing creation and output remains static so that the information trail from layout, to drawings, to output format can be followed systematically. The same board can be viewed from the top or bottom on the same drawing page, with different layer sets per view. If the board changes, a simple update can be triggered so that new drawings can be output.

How the EDA Design Automation Nation is Evolving Today

All in all, automating PCB design is moving in the right direction. The days of ground breaking new PCB software options are slowing slightly with the maturation of the market, allowing for more robust options to be incorporated into the existing infrastructure of the EDA software environments. For Intercept, this has allowed further exploration into their specialty design options for hybrid and RF design. Pantheon and Mozaix were recently enhanced to offer brand new, up-to-date ink resistor generation, answering a need for very precise and accurate ink configurations on hybrid and RF boards.

Intercept is also keeping a close focus on devices and operating systems, such as the proliferation of Apple laptops in EDA workplaces. Making software available on any operating system and through whatever device users want to use will be important going forward, and may even change the dynamic of how software is developed overall. The management of raw code across many different operating systems is not trivial.

The movement of the PCB layout world toward MCAD systems is continuing forward at a decent pace as well, with 3D modeling systems working more closely with MCAD to model boards and identify problems quickly in the de-



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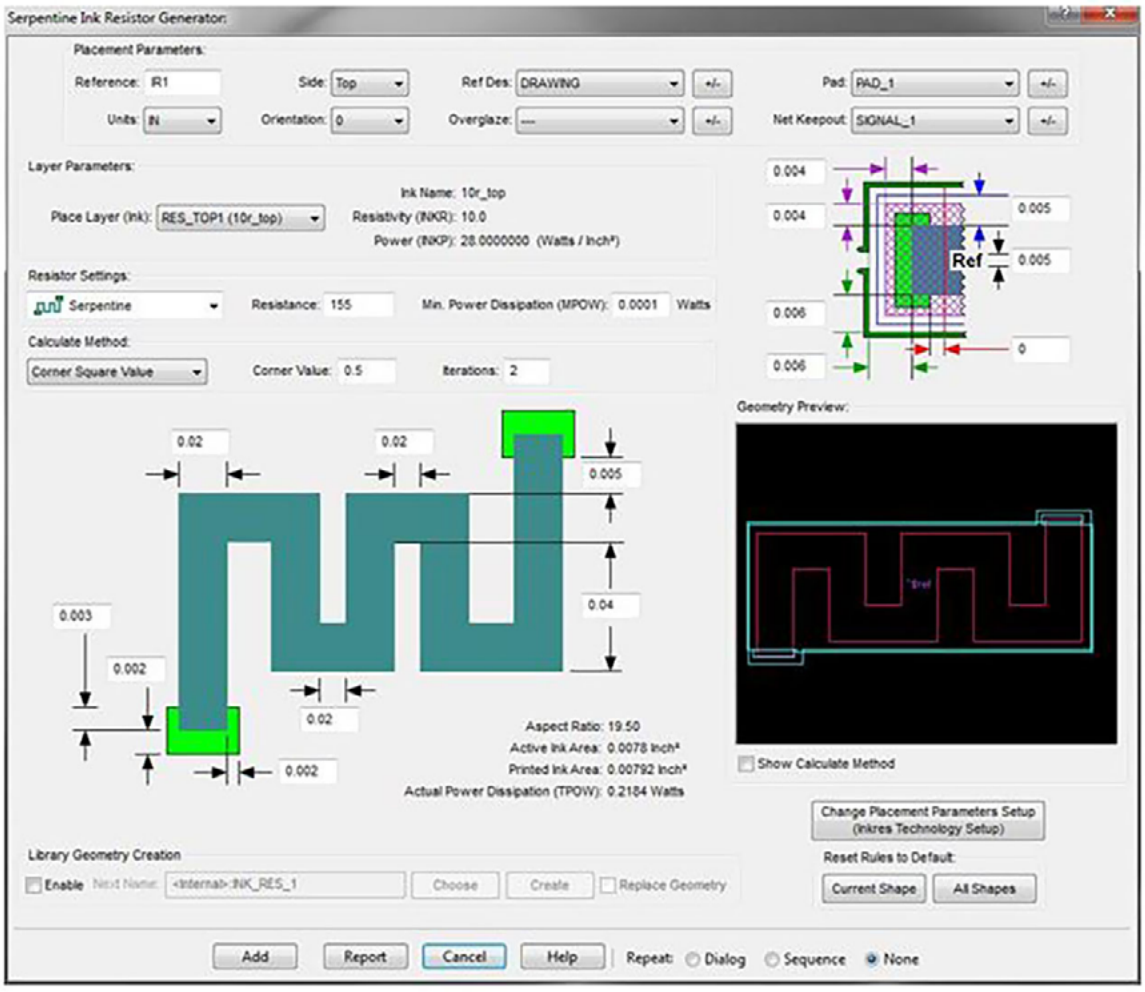

Figure 8: As ink resistor technology continues to become more prevalent in PCB designs, Intercept answers the need in its Pantheon layout application with its brand new, up to date Ink Resistor Generator.

sign phase. But sometimes the added productivity of this movement can be questionable, since STEP model support and setup is not always as automatic as it is said to be. Since the MCAD department will still require its own analysis and approval, and still uses its own native systems, it remains to be seen how the marriage of PCB to MCAD will play out.

As for the approach EDA software vendors are taking to these topics and so many others that encompass our world of automation, the most successful is through the tabulation of information gleaned directly from the users. At Intercept, we keep close tabs on the pulse of information, from social channels all the way down to support channels. Areas of frustration are important to listen to, but there is magic in the resounding silence received when an enhancement is a success among users. EDA vendors must have open eyes and ears at all times. **PCBDESIGN**

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Abby Monaco, CID, is with Intercept Technology Inc. and has 15 years of experience in EDA. This article was written in collaboration with Downstream Technologies and Polar Instruments Inc.

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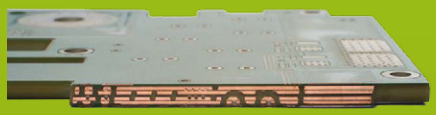

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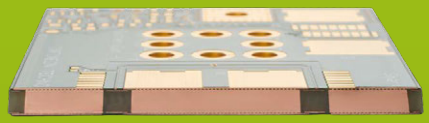

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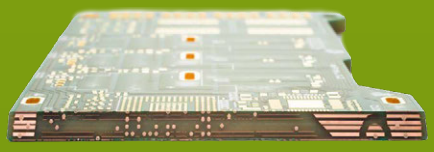

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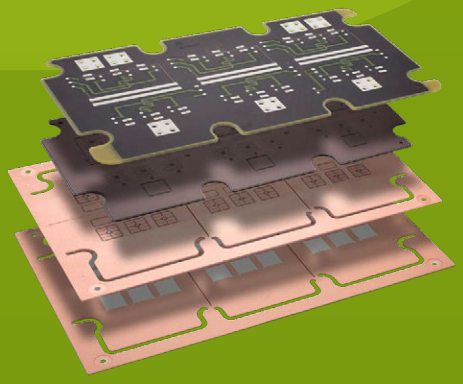

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The Case for Artificial Intelligence in EDA Tools

by Barry Olney
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I-Connect007 Editor Andy Shaughnessy reported that the keynote speaker at the IPC APEX EXPO Design Forum was Dale Parker, a former PCB designer at Shure who is now a CAD manager at Google X. Parker is involved in the development of autonomous vehicles and all sorts of other great ideas at Google X. According to Andy, Parker told the crowd, among other things, that EDA tool vendors need to trash all their old 1990s code and start over, this time with artificial intelligence.

There has been a lot of activity in the field of AI recently, with such developments as voice recognition, unmanned autonomous vehicles and data mining to list a few. But how could AI possibly influence the PCB design process? This month, I will take a look at the endless possibilities.

So much time is wasted on reproducing the same thing over and over again on each layout. Current EDA tools, with all their bells and whistles, are still very limited in automation processes and mostly rely on the skills and foresight of the engineer and PCB designer to drive the software through all the hoops. Instead, EDA tools need to predict what the designer is trying to do, then look at previous designs to suggest alternatives and auto-complete the design where possible. AI is a system that perceives its environment and takes actions to maximize its chances of success.

Automating many of the tedious steps in setting up the initial database would be a good start. A standard form factor could be used to establish the initial layout environment ensuring that designs are compatible across multiple generations of technology. Although some PCB layout tools allow the designer to load a standard set of predefined startup configuration files, there is still too much manual intervention required. The PCB database could predict the fundamental design rules and via stack requirements sourced from previous experience.

Figure 1: Artificial intelligence is part of the future of EDA tools.

Predictive text, which we all use every day on our cell phones, could provide self-evident naming conventions for supplier part numbers and database fields, greatly speeding up the design definition. Busses and interfaces could be analyzed and categorized with naming conventions interpreted from the chip pin name assignments, eliminating much of the monotonous schematic capture process. IC power pins could have powers supplies assigned based on datasheet requirements. And a starter set of decoupling capacitors, added to each power pin, could kick off the PDN analysis

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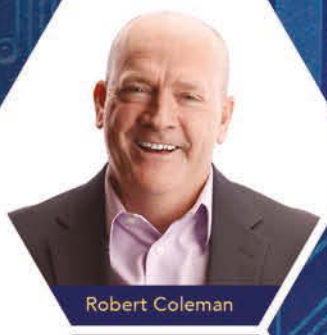
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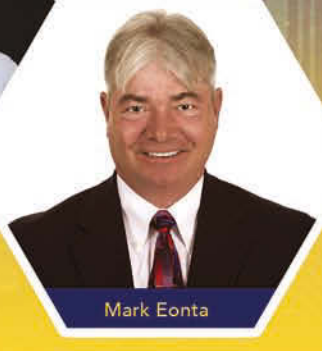
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based on previous capacitor availability and parameter selections.

A selection of predefined library components could be offered, based on an initial bill of materials, and pre-placed on the schematic predicting the designer's requirements. IBIS models could be automatically assigned to each chip, based on the part number and all the interconnecting transmission lines identified. The IBIS model's source and load impedances could be extracted to assign the required impedance and terminations to each individual transmission line.

Also from this, the board stackup could be created based on previous designs, with similar technology, selecting dielectric materials, from a well maintained library, sourced from the preferred fabricator availability, dielectric loss and bandwidth requirements. Data and address busses together with clock/strobe different pairs, defined at the schematic entry level, could be assigned to certain layers in order to minimize crosstalk, electromagnetic emissions and return path loops. Power plane shapes could be automatically defined based on component placement and on the pins that need to be connected, allowing for DC drop and maximum current supply.

Memory blocks—whether they be synchronous, asynchronous, source synchronous, clock-forwarding or embedded clock—could be recognized and standard design rules deployed. Busses and interfaces could be also analyzed and recognized. The entire design rule set could be built from a combination of these requirements and those learnt from previous similar designs.

Functional blocks that the designer is working on, could be scrutinized in order to anticipate which blocks might be useful in future designs and these could then be made available to other designers on the corporate intranet. A database of reusable placement and routing blocks could be made available so that the intelligent database can readily identify a suitable block to drop into the design–the selected block could then be automatically adjusted to the specific needs of each instantiation.

Intelligent forward and back annotation would be a definite godsend. Traditionally, the schematic capture and PCB layout software were developed as separate applications coupled by the annotation process. Why can't we have a common database for both schematic and PCB totally eliminating the constant need to update in one direction or the other? When an ECO is implemented on the PCB, the schematic should instantly know and understand the changes and vice-versa. Over the years, forward and back annotation has been one of the most frustrating and time-consuming issues.

The intelligent database could suggest placement of critical components based on the established design rules, matched delays of busses and define routing strategies based on the technology used. But, will autonomous routing ease PCB gridlock? Placement changes could be

Figure 2: SMT assembly production line (Courtesy Juki).

made to open routing channels and land sizes adjusted automatically to ease routing based on design rules. The AI router could decide which layer and direction to route a bus in order to alleviate bottlenecks that generally occur in the center of the board.

The PCB project deliverables such as Gerber, IPC-2581B or ODB++ and pick-and-place files could be automatically generated based on the established design constraints. Fabrication documentation could also be auto-completed based on established standards.

On the assembly side, Internet of Things (IoT) manufacturing is currently being deployed. This system supports live bidirectional data flow between all electronics manufacturing shop floor machines and processes creating a "smart" factory with "plug and play" deployment. This allows an organization to overcome the bottleneck of establishing efficient machine-to-machine and machine-to-human communications.

I'm sure both you and I could come up with many more ideas to intelligently automate the PCB design process if time permitted. And although such a tool is many years off, the concept behind the EDA AI tool looks promising. PCB designers can certainly use all the help they can get. And, having the design tool intelligently automate their work flow could substantially speed time-to-market.

However, there is already considerable resistance to AI with some suggesting it many create too many erroneous results to be useful, and cannot be trusted. There is also the potential downside that AI might work too well and reduce the skill level needed for the role of the designer to simply indicating the goal and examining the results—but that is a long way off!

Points to Remember:

- Dale Parker, CAD manager with Google X, said in his Design Forum keynote that EDA tool vendors need to trash all their old 1990s code and start over, this time with artificial intelligence.
- Current EDA tools, with all their bells and whistles, are still very limited in automation processes and mostly rely on the skills and foresight of the engineer and PCB designer.
- Automating many of the tedious steps in setting up the initial database would be a good start.
- Predictive text could provide self-evident naming conventions for supplier part numbers and database fields greatly speeding-up the design definition.
- A selection of predefined library components could be offered, based on an initial bill of materials, and pre-placed on the schematic predicting the designer's requirements.
- The IBIS model's source and load impedances could be extracted to assign the required impedance and terminations to each individual transmission line.
- The board stackup could be created based on previous designs with similar technology.
- Functional blocks that the designer is working on, could be scrutinized in order to anticipate which blocks might be useful in future designs.
- Intelligent forward and back annotation would be a definite godsend.
- Placement changes could be made to open routing channels and land sizes adjusted to ease routing based on design rules.
- The project deliverables such as Gerber, IPC-2581B or ODB++ and pick and place files could be automatically generated based on the established design constraints.
- IoT manufacturing is currently being deployed creating a "smart" factory with plug and play. **PCBDESIGN**

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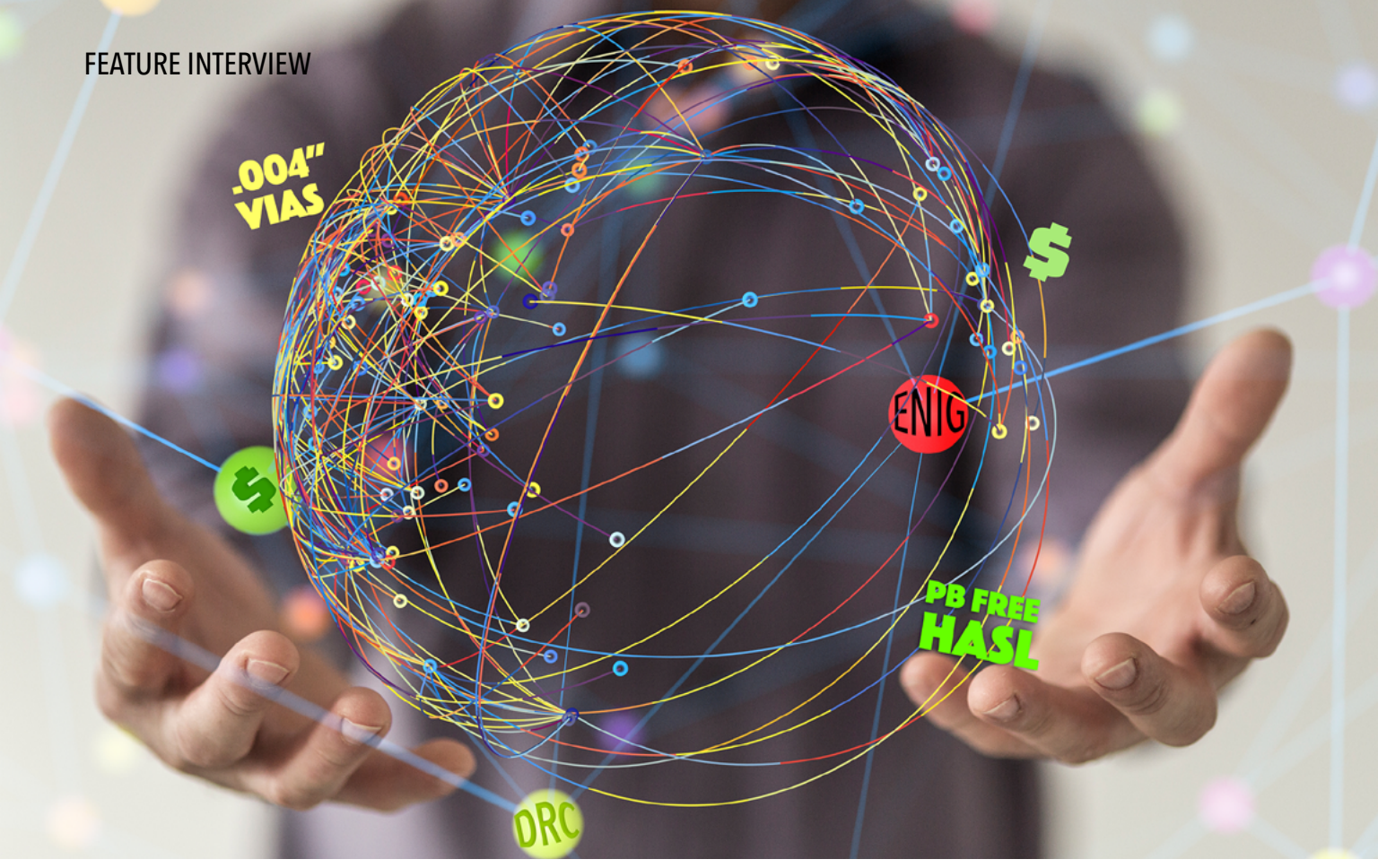
Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.



Design Automation Tools, Today and in the Future

by Andy Shaughnessy

Kelly Dack has been designing PCBs for over three decades, at OEMs of all kinds. Now a PCB designer with a Washington state contract manufacturer and a certified trainer with EPTAC, Kelly enjoys waxing philosophic about PCB design and design automation in general. I asked Kelly to answer a few questions about the direction EDA tools are headed, and whether he'd like to see more control, or more automation in his PCB design tools.

Andy Shaughnessy: *You've been a PCB designer for quite a few presidential administrations, shall we say! In general, what do you think of today's design automation tools?*

Kelly Dack: I've heard them described by different designers as just different sets of hammers, in that they all get the jobs done. That classic metaphor might need to be modified a bit. Take for instance a modern roofing hammer. With the help of a nail gun, utilizing pneumatics and standardized nails on reels, hammering a shingle onto a roof is now highly automated. The tool systems can be very effective, but often with automation can come frustration. My sister Karin recently purchased a nail gun to re-roof her garage. The gun kept jamming so she returned it to the store and came back with a different model. It worked for a while but then it jammed too. She ended up having to try different nail types and even exchange the gun again for a different brand in order to finish her roof. Any old timer watching the job would have said, "I could've had that job done with an old fashioned hammer by now."

I think this story could be considered metaphor for PCB design automation today. Design automation requires a consistent application and vision, budget, time, trial and error and repetitive need in order to be considered an efficient PCB design solution.

Shaughnessy: *For your day-to-day design work, would you rather see more automation in your tools, or have more manual control? Is it just a matter of having the correct mix?*

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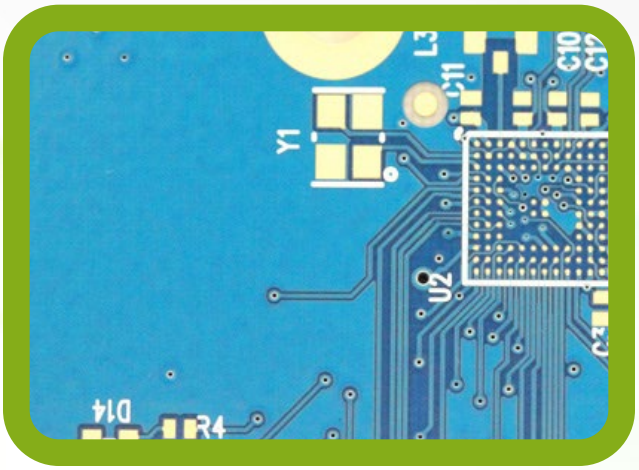

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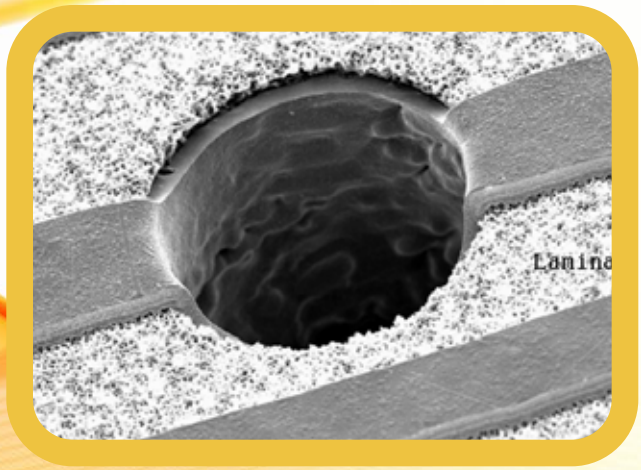

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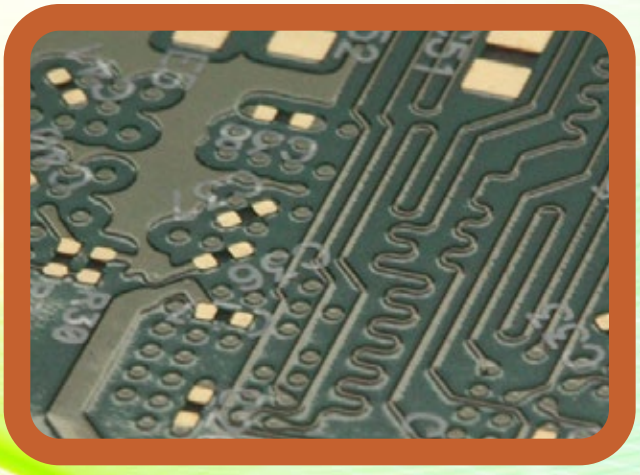

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Kelly Dack

Dack: Great question and I can stick with the same metaphor. Like my sister had the vision to see her garage roof quickly finished using an automated tool, I'd love to be able to slam out board designs using more automation. But as my sister needed to pull out the compressor, order special nails, run the hoses and replace equipment before ever starting the job, the PCB design automation strategy for a particular job may not be worth the effort. Just because we have automation tools we should not be obligated to use them unless they really improve the task at hand.

Shaughnessy: *In what areas of design do you usually favor more automation?*

Dack: Repetitive processes and processes prone to human error. The CAM output routine is a simple example. The software I use allows me to set up a CAM output file routine and hit start. The two-layer, four-layer, and six-layer jobs I do usually have consistent stackups so pre-programmed routine works well. Unless it doesn't. But because my process is consistent it is easy to find where the process the error occurred. I find that output errors usually occur with something inconsistent in the design; unique patterns of associated copper that must be switched on, etc. To facilitate automation I find myself striving to be more consistent in my design methodologies.

Shaughnessy: *For what tasks do you prefer having more manual control?*

Dack: Just to be clear, any preference for manual control is based on a deficiency or performance problem in automatic mode. Also, when I route. In fact, always while routing. Did I mention that I like manual control while I'm routing? Also, library part manipulation. I prefer the types of tools that allow the user to edit a part decal on a board interdependently of the library—without having to save it to the library. This allows for the odd times when the legend really needs to stand out or one land needs to be modified to adapt to a custom processing situation.

Shaughnessy: *In one survey we did, about 15% of designers said their EDA tools take away too much control. Do you understand their position?*

Dack: It would be interesting to see how those stats match up to percentage of designers laying out simple designs vs. complex designs. Working recently with a busy PCB fabricator in Seattle and a now a high-quality electronics contract manufacturer, I have seen quite a variety of designs that are very good but need minor manipulations to optimize them for manufacturing. The edits should be able to be performed in a matter of minutes. But if the layout tool requires hand-shaking with the schematic in order to move forward without "breaking," well, the layout won't move forward until the schematic is in synch. Makes sense, except when the schematic responsibility and deliverables are owned by the EE or the part decal is owned by a component librarian and are required to be fully checked and approved before being passed to the designer for use. This has the potential to slow the prototype design cycle and time-to-market down considerably.

Shaughnessy: *How often do you use an autorouter? If not, why not?*

Dack: Never! Are you surprised? This question has been asked of the design community for a long time. It is only the designers who are doing layouts with repetitive circuitry that will benefit from the time that it takes to set up the autorouter's constraints. I recall using autorouters in the late '80s and early '90s when DIP style IC memory boards were large and low speed. These were the golden years of the autorouting. The boards were consistent and very predictable. Today, I use the heck out of "dynamic" routers. Tools that allow the designer to interactively route a line or group of lines while steering the cursor in the preferred direction. Interactive modes will automatically push and shove and plow the selected lines adhering to set design rules constraints. If a problem arises, the DRC can be interactively manipulated to ease the constraint if required.

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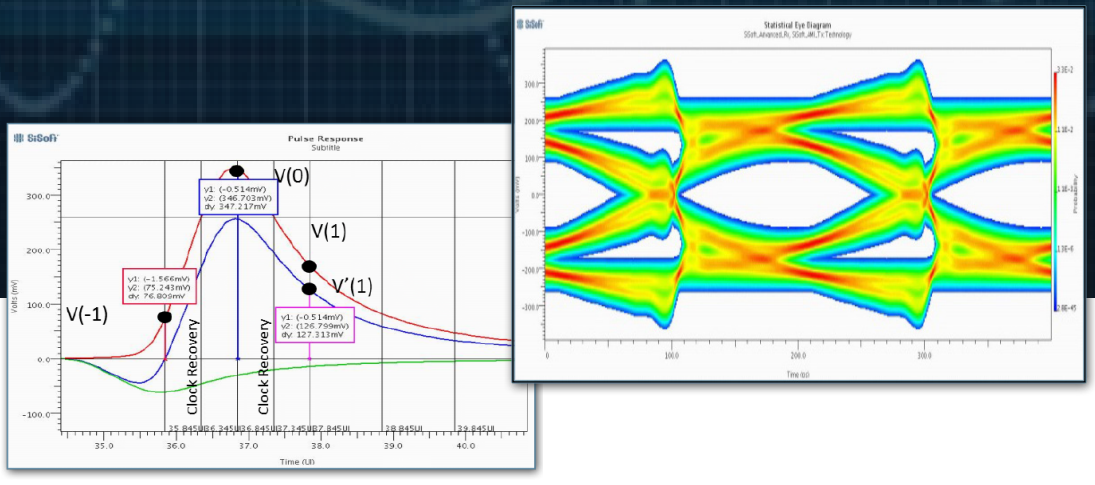

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Shaughnessy: ***Do you utilize your tool's design reuse capabilities?***

Dack: Again, reusablilty is dependent on design. Many success stories of designers utilizing true reuse repetitive environments, but automatic design reuse is constrained by so many things: layer count, reference designators, etc. Reuse can require setup and agreed upon reference designators and layer counts. A lot of set rules are required between the EEs and designers or success will be limited. For simple, repetitive channels on a board, I find that using a simple "copy" routine can work very effectively.

"Reuse can require setup and agreed upon reference designators and layer counts. A lot of set rules are required between the EEs and designers or success will be limited."

Shaughnessy: ***Do you perform post-processing and documentation manually, or use a tool such as DownStream?***

Dack: I have great things to say about DownStream's BluePrint. I'd probably say great things about any other automated doc tools too, but there aren't any! DownStream has done a great job of filling this void in the EDA market. DownStream's BluePrint tool is a bonafide cost time/cost saver. I can say that because while working for a Northern Nevada gaming company and pitching the idea of using BluePrint for years, a progressive manager I worked for at the time became interested and we diverted licensing fees we'd been paying for an archaic, manual form of documentation utilizing four peripheral software tools.

After installing BluePrint we reduced our entire PCB documentation time down to approximately 10 minutes! BluePrint leveraged our source database to allow us to manipulate data to specify and document a PCB in ways our source layout program could not. These guys got kudos and two thumbs up not only from me, but our entire team of designers and management as well.

Shaughnessy: ***What current manual tasks would you like to see automated in your EDA tool in the future?***

Dack: How about autoroute and verify based on current carrying capability? The design database has data on copper thickness and width. Let's go to the next step and be able to query current carrying capacity of a conductor! Let's be able to add current carrying constraint to a line in the schematic, route and cross-check to the constraint. Yep.

How about visual cavity creation based on height constraints? How about automated access to any spec that is called out?

How about a manufacturing constraints import? Think of it: component suppliers have provided IBIS models and are now providing step files, maybe PCB suppliers can start providing manufacturing constraints that could be imported into a design. Maybe "dynamic" quoting as the design is being laid out. Can you imagine? Say you start with a basic two-layer PCB—the supplier's sweet spot. Board starts at $600. Then you redefine the board outline and the new price is reflected. Then you add component footprints, and vias without noticing any price change until you add that .004" diameter via. Bing! The price adjusts accordingly. Add a note for lead-free HASL, the price doesn't change. Change the note to ENIG and you see the dynamic quote indicator bump up slightly. With the influx of engineering students and even seasoned engineers performing the layout function, a tool like this would really help these newer folk to become aware of the manufacturing and cost ramifications of the design features they add.

Shaughnessy: ***Thanks for your time, Kelly.***

Dack: Thank you, Andy! **PCBDESIGN**

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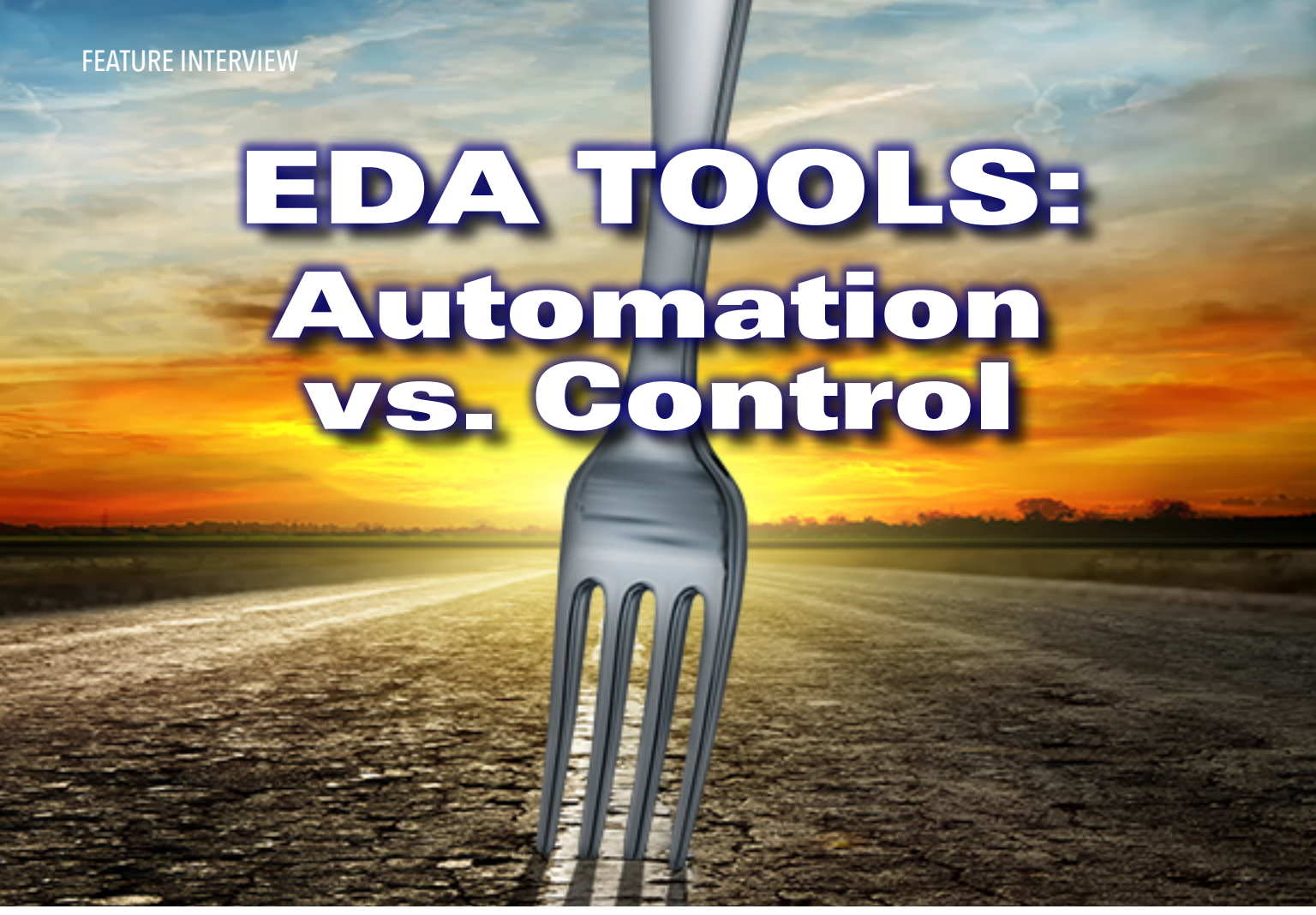

EDA TOOLS: Automation vs. Control

by Andy Shaughnessy

Stephen V. Chavez, CID+, has been a senior-level PCB designer for almost 20 years. He is currently the lead PCB designer for the Electronic Systems Center division of UTC Aerospace Systems (UTAS).

Stephen stays pretty busy. He's the vice president of his local IPC Designers Council chapter in Phoenix, and a Designers Council Executive Board member at large, and he is recognized as a Subject Matter Expert by IPC. He often speaks at the Design Forum at IPC APEX EXPO. At this year's Design Forum, "Steph" spoke about the importance of taking charge of your PCB design education and networking.

I caught up with Stephen and asked for his thoughts on the EDA tools of today, and whether he'd prefer to have more control vs. more automation.

Andy Shaughnessy: *You've been a designer for a few years. In general, what do you think of today's design automation tools?*

Stephen Chavez: It's true that I've been designer for many years now and have used a variety of tool sets. In my experience, I find today's automation tools extremely useful and when the opportunity presents itself to use these type tools, they can assist greatly in the overall success of a project. Today's tools have gotten very powerful. They range from very simple to use, to very complex in nature. In my opinion as a designer, I strongly feel that when a designer progresses in his/her career and perfects his/her craft, if and when the opportunity exist, they should take advantage of these new automated tools to design a more quality product, shorten the overall design cycle, and positively affect the overall project budget. With today's designs getting more and more complex, there are instances where the only way to complete a task is to take advantages of these automation tools. Taking advantages of the horse power within these automation tools in today's design world is key and I feel these tools should be evaluated to see how they can benefit you and your employer by positively impact your effectiveness

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as a designer and ultimately improve your company's success.

Shaughnessy: ***For your day-to-day design work, would you rather see more automation in your tools, or have more manual control? Is it just a matter of having the correct mix?***

Chavez: For me, I'd rather have more automation in my tools. Being able to do tasks faster, work more efficiently, and producing better quality designs allows me more time to evaluate multiple options for better results and of course shortens my design cycle. With that said, having the correct mix is important too. I feel each designer has to figure out what works best for him/her and within his company. In the end, it's not the tool that makes the difference… It's the designer!

Shaughnessy: ***In what areas of design do you usually favor more automation?***

Chavez: For me, I'd have to say the areas of design I favor more automation are as follows: constraint input/edits/updating, autorouting, generating outputs, documentation, DFM checking (Valor), design re-use and library part creation (symbols and cells). These are areas I feel where taking advantage of today's automated tools is a must and can be a game changer.

Shaughnessy: ***For what tasks do you prefer having more manual control?***

Chavez: I'd prefer to have more manual control when importing mechanical data from one tool set to another that contains constraints. An example, IDF files containing many different height restrictions and keep out zones within the PCB outline. Another area I prefer more manual control is during part placement. In this stage, not only am I placing parts on the board to optimize the routing and meeting mechanical requirements, I am actually routing the design mentally in parallel. This way by the time placement is 100% complete and validated with an ECAD/MCAD verification and validation analysis, routing goes rather quickly.


Stephen Chavez

Shaughnessy: ***In one survey, about 15% of designers said their EDA tools take away too much control. Do you understand their position?***

Chavez: As I think about this question, I ask myself: "Of those 15% of designers that feel this way, what tools are they using?" Let's face it, todays tools are much better that tools of the past. Of course, the more expensive tools in the industry today—Mentor Graphics and Cadence—have more automation built in and of course more horsepower. Knowing how to use it is the trick and be willing to trust the tool. As a designer today, you should be willing to trust your tool and learn how to use it to your advantage to be more effective and successful. You can be assured that your competitor is doing this.

Shaughnessy: ***How often do you use an autorouter? If not, why not?***

Chavez: I prefer to use my autorouter as much as I can in every design possible. In some RF designs and in some high power designs, it doesn't make sense to use the autorouter. Early in my career, I would never use the autorouter. I just never trusted the tool that I was using at that time. As I progressed in my career and stepped into lead roles of large design teams, I learned and understood the importance of the overall design cycle. Knowing how today's automation tools can be a huge game changer regarding speed, efficiency and quality. In my opinion, it does make a difference that the tool set that I use—Mentor Graphics Expedition—has an awesome autorouter. You just have to be willing trust the tool and learn to use it to your advantage.

Shaughnessy: ***Do you utilize your tool's design reuse capabilities?***

Chavez: I do utilize the design reuse but not as much as I would like. Working for a large Aero-

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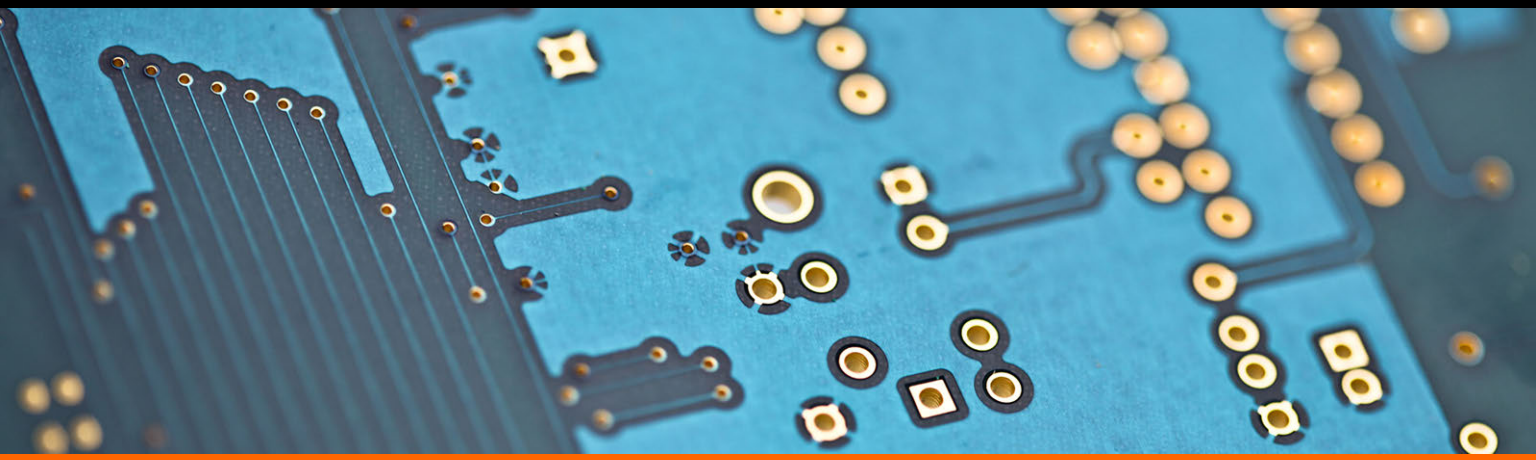

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space company, "reuse" is important. Reuse has to be a full team effort and requires "buy-in" from the EEs to the designers to the librarians to the components engineers. It will save time in design and definitely save time down in the lab when testing out the design since the reuse portion of the design has already been validated. Taking advantage of reuse is a culture that needs to be developed and with today's automation tools, the capability is there. It just needs to be taken advantage of. When reuse is integrated into a design, reuse can be a very powerful asset to you and your company.

"It will save time in design and definitely save time down in the lab when testing out the design since the reuse portion of the design has already been validated. Taking advantage of reuse is a culture that needs to be developed and with today's automation tools, the capability is there."

Shaughnessy: *Do you perform post-processing and documentation manually, or use a tool such as DownStream?*

Chavez: At the Electronic Systems Center, which is the business unit I work for within UTC Aerospace, the electrical designers (ECAD) are closely integrated with the mechanical designers (MCAD). I'd say we have a mix of automation and manual post-processing and documentation steps. We have an integrated ECAD to MCAD hand off process that has been developed and is continually optimized. This process details how ECAD generates certain outputs to MCAD which is who actual creates the final CCA drawing that is completed within a mechanical tool set. All though ECAD is capable of creating a CCA drawing within the Mentor Graphics tool set, Mentor Graphic Expedition is an "electrical tool" for PCB design. In my opinion, it is not a mechanical drawing tool such as NX which is the tool set that our MCAD team uses. I have not had the opportunity to use the DownStream tool but I have some colleagues within the industry that have had good success with this tool and they really like it.

Shaughnessy: *Are there any manual tasks you'd like to see automated in your EDA tool in the future?*

Chavez: I would like to see more options to automate manual tasks on the fly and at the designer's discretion.

Shaughnessy: *What would you like to see in the PCB design software tools of the future?*

Chavez: In today's competitive market, first and foremost, I'd like to see the overall cost of these tool sets come down. As company's look for ways to save in expenses, it's very hard to maintain justification for using these high end tools sets when there are not being utilized to their fullest potential or if there are modules that are required to purchase within a specific toolset and may not be of much use for your actual needs. I would also like to see more of these software tools be willing to integrate better with other tool sets within their same category as well as complementing tool sets and even software such as adobe PDF and Visio for example. As I always state, it's not the tool that makes the difference but rather the designer that does. It's your career and your responsibility to progress, continue to learn, and think outside the box. It's not your employer's responsibility to train you and make you better. It's your responsibility! Where you want to end up in your career is up to you. Just know that with continued education, gaining experience and learning the use of today's automation tool sets, you have the potential to create some great magic!

Shaughnessy: *Thanks for speaking with us, Steph.*

Chavez: Thanks for the opportunity. **PCBDESIGN**

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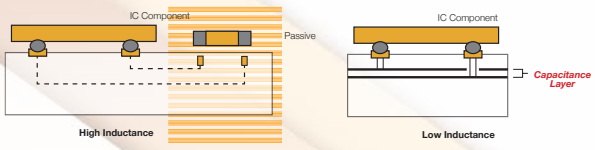

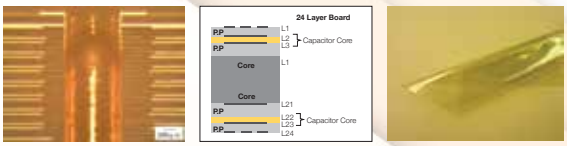

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PCB007 Highlights

Happy's Essential Skills: Failure Modes and Effects Analysis (FMEA)

Failure modes and effects analysis (FMEA) is a systematic process to evaluate failure modes and causes associated with the design and manufacturing processes of a new product. It is somewhat similar to the potential problem analysis (PPA) phase of the Kepner-Tregoe program.

Walt Custer Elaborates on his Annual IPC APEX EXPO Forecast Presentation

IPC APEX EXPO 2016 has come and gone, and this year, Walt Custer's annual presentation forecasting the upcoming year for the industry was much anticipated, as always. I met up with Walt at the show to learn about his presentation and dig deeper into his findings.

IPC President John Mitchell on the Past, Present, and Future, Part 1

We conducted this interview with IPC President John Mitchell on the show floor at IPC APEX EXPO to discuss the event, the changes on the IPC board, and the key metrics that IPC uses to measure their own performance and effectiveness. John also invites the industry to a unique challenge.

American Standard Appoints Dave Olson Vice President of Operations

Anaya Vardya, CEO of American Standard Circuits, announced the appointment of industry veteran Dave Olson to the position of Vice President of Operations.

Weiner's World: March 2016

Sellers of equipment at the Shanghai CPCA event complained of continued poor business. This was especially evident amongst those selling to firms building boards for phones and other portables devices as indicated below. However, not all reports were bad. Major fabricators such as Wu's in China, not dependent upon HDI or flexible products, stated that they were "satisfied" with their current business levels.

Green Legislation and the Impact on Electronic Materials and Processes

In general, "green" and "environmentally friendly" refer to manufacturing that involves the replacement of toxic substances with less toxic materials, the elimination of materials or processing steps, less consumption of chemicals (i.e., more efficient or higher yield processing), reduction of water use, reduction of energy use…

Williams and Beaulieu: Board Shops and CMs Must Communicate Better

Two well-known consultants in the PCB industry, Dan Beaulieu and Steve Williams, have joined forces to try to help close the divide between CMs and board shops. I recently sat down with them at IPC APEX EXPO 2016 to better learn about their strategy for bringing the two sides together.

IPC President John Mitchell on the Past, Present, and Future, Pt. 2

In Part 2 of our on-the-show-floor interview with John Mitchell, conducted at IPC APEX EXPO 2016, John continues describing IPC's key measures, and then invites industry folks who are reading this to participate in a unique challenge—some might say experiment. The question is, will there be any takers?

Rep. Mike Honda Visits Bay Area Circuits' California Facility

"I am grateful to Bay Area Circuits for hosting me today," said Congressman Honda. "It's great to hear from the employees that have played a vital role in the company's success. It's a reminder of the contributions they make to this country's and California's economy."

The Sum of All Parts: Total Concept—Growing for the Future

Last month, we discussed the importance of the PCB industry's need to focus on a "made in USA" philosophy. This month, we will go over how to methodically do this amid different company cultures and different logistical challenges.

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The Basics of Hybrid Design, Part 3

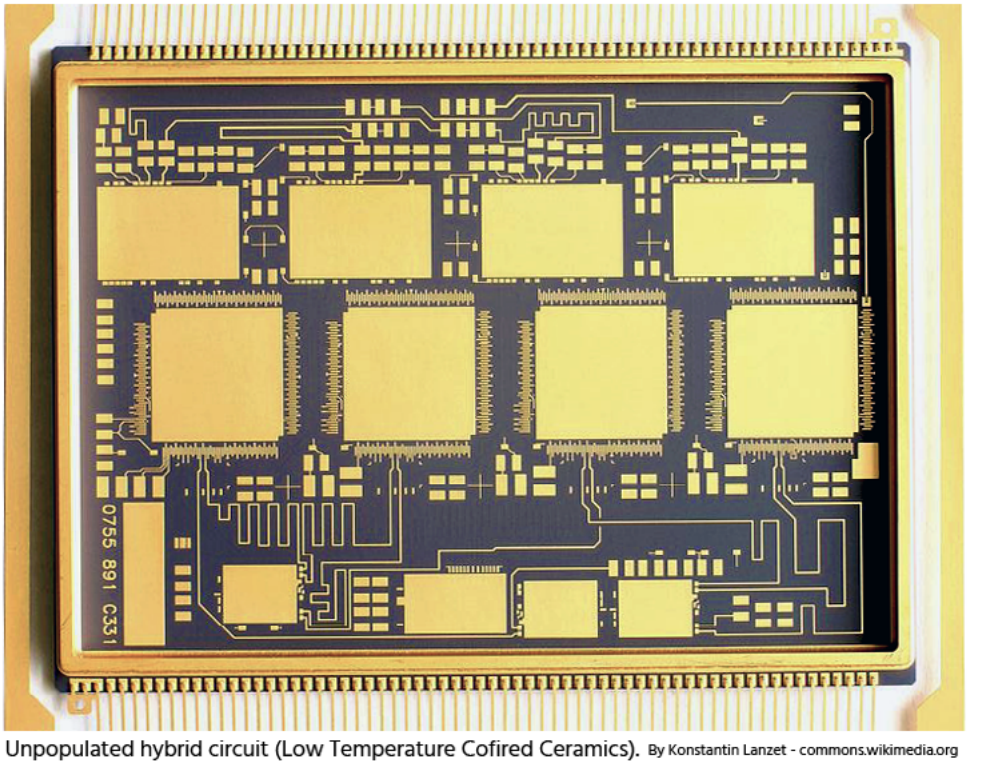
by Tim Haag
INTERCEPT TECHNOLOGY

In the first two parts of this series, we discussed the basics of hybrid design from the PCB designer's perspective, and this month we will conclude that discussion.

We are seeing more and more of our customers exploring the world of hybrid design, and we are getting new customers for whom hybrid design is their sole focus. The world of hybrid design is growing, and we have lots of hybrid-specific functionality built into our software that helps designers meet and conquer the unique hybrid design requirements that they are faced with.

And yet many designers out there (and I used to be one of them) have no idea what is meant when people start talking about hybrid design. It is therefore not uncommon for designers to avoid the subject directly while hoping to pick up little cues and pointers from others indirectly so that they are no longer in the dark. If that description sounds uncomfortably close to where you are at, then read on. My hope is that this three-part series will help you by serving as a basic introduction into the world of hybrid design.

If you haven't had a chance to read the first two parts in this series, please go back to the last two months and take a look at them if you can. To summarize, however, we discussed in the first column the basic structure of hybrid designs and the benefits they offer over standard PCBs. In the second column we discussed some of the similarities and differences in CAD applications for the design of hybrids and how hybrid designs and their layer stackups are setup. We also discussed the routing of conductors (wires), and the creation of area fills and power planes. We continued from there talking about the creation of dielectric layers and their similarities and differences to fills and planes. Next we introduced the concept of cross-over dielectric layers, which is unique to hybrid designs,



Unpopulated hybrid circuit (Low Temperature Cofired Ceramics). By Konstantin Lanzet - commons.wikimedia.org

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and how they are used. Finally we finished up with an explanation of how vias are created and managed in hybrids. Now, let's talk about components.

The selection of components in a hybrid design is influenced by the operating temperature of the working design. Higher operating temperatures will require components that can withstand those extremes while at the same time necessitating a different amalgamation of soldering elements for manufacturing.

Passive components will use packaged parts while active components will use bare dies (no packaging). This is something different for the PCB designer who would rarely see a bare die used on a board design. Packaged active components can be used on a hybrid, but this is dependent upon the operating temperature of the design. And by using bare dies, a hybrid design realizes the benefits of shorter circuit paths, smaller size, and better thermal conditions for the device as it is glued directly to the substrate making for a better heat sink.

> "Passive components will use packaged parts while active components will use bare dies (no packaging)."

There is also another benefit to using bare dies over packaged devices: wire bonding. The connectivity points on a bare die are on the top of the die and in order to connect to the connectivity points of the substrate circuitry, little gold or aluminum wires are bonded between the connection points during the manufacturing process. Although this is a labor-intensive operation, it does have its advantages. Since the connectivity points on the substrate circuitry can be moved, the hybrid designer can organize the design in order to optimize the connection path. Imagine on a PCB if you could move the pins of an IC to wherever you wanted to in order to improve the routing channels. Well, on a hybrid design you can do just that with the wirebonds.

Hybrid design CAD applications have built into them the ability to move the wirebond land patterns (connectivity points) on the substrate. The designer also has the ability to rotate the land pattern (which is usually an oblong shape) in order to match the angle of the wirebond. Wirebonds are routed between the connection points in the same way that a regular conductor is routed. Also, the wirebond is routed from a net guide just as you would see on a PCB when routing a trace. Once routed, the wirebond itself will show up in the CAD application as a differently colored wire that is displayed on a different CAD layer in the application.

The wirebond is an intelligent net object just as a conductor (trace) is, so that net rules and connectivity lengths can all be analyzed and accounted for within the CAD application. And in addition to that, wirebonds can be assigned their own unique reference designators as well as height properties to assist in the manufacturing process. They can also have DRCs run on them to check for spacing violations. Additionally, wirebonds can be used as a regular conductor (wire) connection on the substrate if needed. This gives the designer the ability to connect a net that there isn't room for on a regular layer in the substrate. In this way the designer may be able to prevent the printing of an additional conductive layer for just a few extra connections.

There is yet another type of component that is unique to a hybrid design, and that is the ink resistor. An ink resistor has some distinct advantages to it over using a standard SMT component resistor. Ink resistors can reduce cost by eliminating the need to maintain a stock of similar packaged parts. They also can be laser trimmed for a precision tolerance which makes them more cost effective than finding and using component mounted resistors having the same tolerances.

The creation of an ink resistor starts in the schematic where the required resistance value is designated. This information is forward annotated into the layout of the hybrid where

the CAD application automatically creates an ink resistor shape using its dynamic parametric ink resistor generator. The CAD application has within it several layers representing different values of ink, and the generator will choose the appropriate type of resistor ink from those layers. Then the generator will dictate the size and shape of the ink resistor according to the values specified by the schematic. At any time though, the designer can manually override these settings to change the layer, size and shape as required.

The parametric ink resistor part within the hybrid CAD application will also carry with it all the attributes needed for its creation. These include; overlapping of resistor ink over the connecting pads, the specific value of ink used (e.g., 10, 100, 1000, 10k, 1m, etc.), layer trimming, laser trimming, and overglaze information. And as mentioned before, these values can be manually altered by the designer to fit any unique size and shape requirements of design. By changing an ink resistor using the dynamic parametric ink resistor generator of the CAD application, the designer will assure that the final ink resistor will still carry the required resistance values that it should. For example; the parametric ink resistor generator will increase the width of the ink resistor proportionally if the designer should decrease the length, etc.

The remainder of the hybrid design process is going to be very similar to what the PCB designer is used to. DRCs will need to be run, silkscreen and documentation will need to be created and finalized, and the manufacturing files will need to be generated. And then…congratulations! You have successfully made it through your first hybrid design and although scary, you got the job done. And with that, our series on the basics of hybrid design is concluded. There is certainly much more that we could talk about in the creation of hybrids, but let's save that for another time. For now though, we've walked you through the basics and my hope is that you now have a better grasp on this new and exciting arena of hybrid design.

And before I leave you, I want to once again give a shout-out to my colleague Bernd Pflueger. Bernd has a tremendous depth of knowledge and experience in the world of hybrid design, and I am extremely grateful for his help with this series. **PCBDESIGN**

Tim Haag is customer support and training manager for Intercept Technology.

Small and Powerful: Pushing the Boundaries of Nano-Magnets

Researchers have created extremely small, thermally stable magnetic particles. These CoFe2C nanoparticles have magnetic properties comparable to some rare earth magnets, the strongest permanent magnets ever created, at sizes as small as 5 nanometers, a million times smaller than an ant.

The next generation of thermally stable data storage devices demands materials that are highly magnetic in a specific direction at small particle sizes. The new CoFe2C nanoparticles accomplish this goal and can lead to nano-magnets that work at room temperature.

One of the greatest problems hindering the field of nano-magnetism is that small particle sizes tend to mean small magnetic anisotropy. A large magnetic anisotropy is absolutely crucial to these nanoparticles because it prevents fluctuations of the magnetic moment, a phenomenon that limits the use of these particles in memory storage and many other applications.

To become technologically relevant, nano-magnets must be small, have a large magnetic anisotropy, and be thermally stable. Researchers at Virginia Commonwealth University have computationally investigated CoFe2C nanoparticles with mixed CoxC and FexC carbide phases that fit this exact description. After promising theoretical results, the researchers successfully synthesized the CoFe2C particles with the properties that were computationally expected. The newly synthesized particles have been proven thermally stable up to 790K at sizes as small as 5 nanometers.

These CoFe2C nanoparticles possess the unique characteristics of both small size and a large anisotropy, and could represent the future of data storage devices.

Coatings: Five Essentials for Designers

by Phil Kinner
ELECTROLUBE CONFORMAL COATINGS DIVISION

As I sit down to write my fourth column on the subject of conformal coatings, I'm reminded—as we in the UK continue to experience almost sub-arctic weather conditions this Spring, including snow in April—that it is always best policy to be prepared for those unexpected environmental elements. And where electronic circuit board protection is concerned, that means being prepared for all eventualities. So, as the central heating is fired up a notch or two and the barbecue stove is wheeled back into the garage, let's consider what we've covered so far on the subject of conformal coatings.

True to form, I'll be providing five PCB design pointers each month to help you avoid some common pitfalls when applying conformal coatings. We have so far looked at tricky production related issues that could so easily have been resolved at that all-important design stage, examined some of the more common dos and don'ts; those issues that come up time and time again, despite meticulous attention to design detail, and which must be taken into consideration when coatings are finally applied. We've explored the implications of housing design on conformal coating performance, particularly the influence that fixtures and fittings can have in terms of thermal shock loading and the adverse effects of forced air cooling when abrasive particles are present. So for May, let's cover how the physical shape of board components and the interaction with solder paste, solder masks and fluxes can affect conformal coating integrity.

The focus for this month will be my absolute essential facts—my "Never leave home without them" list, so to speak!

Fact 1: In an ideal world, PCB designs would not have an inherent weak point for corrosion; unfortunately, in the real world, they do. A really neat way of determining this weak point is to use stress tests such as powered condensation tests. When a weak point is revealed, you are

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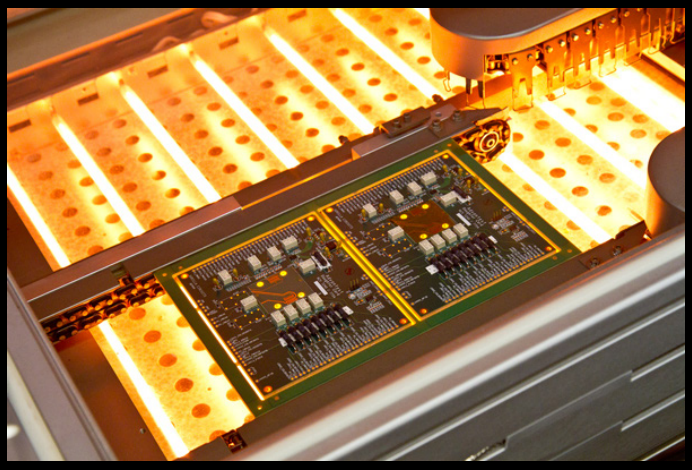

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better equipped to deal with it. Often the spacing of components, board finish and distance to ground planes can be optimised for corrosion resistance.

Once the design is optimised for corrosion resistance, the conformal coating will often be even more effective in ensuring corrosion free operation. Stress tests (thermal shock, for example) are not intended to be used on final assemblies for product validation. Failure mechanisms may well be different, and may be missed by stress tests. Product validation testing should mimic end use environments as closely as possible. (Here at Electrolube, our testing is designed to push products even further than in actual usage scenarios.)

> "Failure mechanisms may well be different, and may be missed by stress tests."

Fact 2: If you assume that a conformal coating will be necessary from the very beginning of the process, you will not go far wrong. Plan for this, design for this and test for this. You can bet your life that a coating will be required and by factoring this into the design process, it will have the knock on effect of simplifying the manufacturing process and you will have a happy team.

Fact 3: We would all love a universal all-singing, all-dancing coating but life is not like that. Conformal coating is always a compromise and there is no fixed solution, so plan ahead and bear this in mind. Why not have two or three internally approved and tested materials at your fingertips? This will allow you the freedom of choice and will ensure that you can select the best one for the environment in mind, rather than the one that is used the most or the operators prefer using; after all, the most familiar or popular is not always the best for your application.

Fact 4: Technical specifications and standards give a warm fuzzy glow, but the use of a MIL spec conformal coating does not in itself guarantee the coating will perform well in your application! The coatings are tested on a flat, bare FR-4 substrate, without solder mask, flux chemistry or the effects of multiple thermal excursions. A key tip is to obtain the MIL document and familiarise yourself with the test conditions and properties tested and remember the standard is a guide, intended to prevent truly unsuitable coating materials from being considered by the end user. The MIL spec doesn't really distinguish between materials or explore the areas of use for which they might be suitable.

Fact 5: Make sure you check the boilerplate language contained within your drawings to ensure it is appropriate and relevant. For example, MIL-I-46058C was declared inactive for new designs in 1999. However, it still remains "active" due to the boilerplate language that requires a MIL-I approved coating that has been propagated onto new drawings produced since 1999.

I'm very keen to learn if any of the recommendations and hot tips offered in my columns over the past few months have been put into effect by readers, as it would be great to have some feedback from you and hopefully some good news about transforming your process. If you have found my design tips useful and have achieved some success through their implementation, let's hear about it! Sharing your experiences with fellow readers—if you are at liberty to do so, of course—can only have a positive impact on our industry, so spread the word.

In the meantime, I'll do some "coating" of my own and pull on an extra layer of clothing! Roll on summer. **PCBDESIGN**

Phil Kinner is technical director For Electrolube's Conformal Coatings Division.

2016 Programs

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May 19
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September 24–30
IPC Fall Committee Meetings — Meeting
Held in conjunction with SMTA International
Rosemont, IL USA

September 26
EMS Management Meeting — Meeting
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October 19
IPC Education Online — Webinar
Wisdom Wednesday — for IPC Members ONLY
30 minutes of FREE technical insight
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October 25–27
IPC-SMTA Cleaning and Conformal Coating Conference — Conference
Chicago, IL USA

November
IMPACT Europe 2016 — Meeting
Brussels, Belgium

November 2
PCB Carolina: Regional Trade Show — Conference and Exhibition
Presented by the RTP Chapter of the IPC Designers Council
Raleigh, NC USA

November 2–3
IPC Technical Education — Workshop
Held in conjunction with PCB Carolina
Raleigh, NC USA

November 7–11
IPC EMS Program Management Training and Certification — Certification
Chicago, IL USA

November 16
IPC Education Online — Webinar
Wisdom Wednesday — for IPC Members ONLY
A Vision for the Industry

December
IPC Education Online: Winter Semester — Webinar

December 7–9
HKPCA International Printed Circuit & IPC APEX South China Fair — Conference and Exhibition
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IPC Education Online — Webinar
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MilAero007 Highlights

Zentech CEO Matt Turpin Recognized at IPC APEX 2016

Zentech Manufacturing Inc. is pleased to announce that our CEO and President, Matt Turpin, was named as one the electronics industry's Rising Stars by IPC at the recent IPC APEX EXPO in Las Vegas, Nevada.

Catching up with...PNC: Open House Planned for May

I'm a great believer in open houses. Any time customers and vendors get together to learn and talk about what they can do for each other it's a good thing. That's why, when I heard that PNC, in Nutley, New Jersey, planned to hold an open house on May 20, I wanted to learn more about it. So I called my friend Sam Sangani, the company's owner, to learn more about it.

Northrop Grumman Awards Radar Contracts to Kitron

Kitron has been selected as an international source for manufacturing of a sub-assembly related to the JSF Radar system developed by Northrop Grumman Corporation (NYSE: NOC) for the F-35 Lightning II.

All Flex Launches Online Heater Design Course

All Flex announces the launch of an online flexible heater design course that provides technical information to the engineering community. This useful tool self-educates about the design requirements for polyimide and silicone rubber heaters.

Novel Miniaturized Circulator Opens Way to Doubling Wireless Capacity

Researchers have developed a microelectronic substitute for larger-scale magnetic components and opened a pathway to more efficient communications and more capable radar systems.

Newbury Electronics Supports NOC to Discover More about the Deep Sea

Newbury Electronics' connection with the National Oceanographic Centre (NOC) in Southampton started in the early 1990s. Since then both the research science and PCB manufacturing processes have made considerable advancements but Newbury Electronics has kept pace with the scientific demands and continues to supply an extensive range of bespoke boards to the NOC, an internationally renowned research organisation.

NASA Begins Testing of Revolutionary E-Sail Technology

Testing has started at NASA's Marshall Space Flight Center in Huntsville, Alabama, on a concept for a potentially revolutionary propulsion system that could send spacecraft to the edge of our solar system, the heliopause, faster than ever before.

Missile System Would Greatly Increase Defense Capability in South Korea

Right now, the United States and South Korea are in discussions regarding the feasibility of deploying a Terminal High Altitude Area Defense, or THAAD system there, along with its associated radar, while nearby China has voiced objections to the idea.

Program Aims to Facilitate Robotic Servicing of Geosynchronous Satellites

Servicing vehicle jointly developed with a commercial partner would leverage DARPA's successes in space robotics and accelerate revolutionary capabilities for working with satellites currently beyond reach.

DoD's Focus on Increased Training a Boon for Military Technology Market

The Department of Defense (DoD) training and simulation budget is expected to increase throughout the fiscal years defense plan (FYDP) to compensate for the previous years' training shortfalls.

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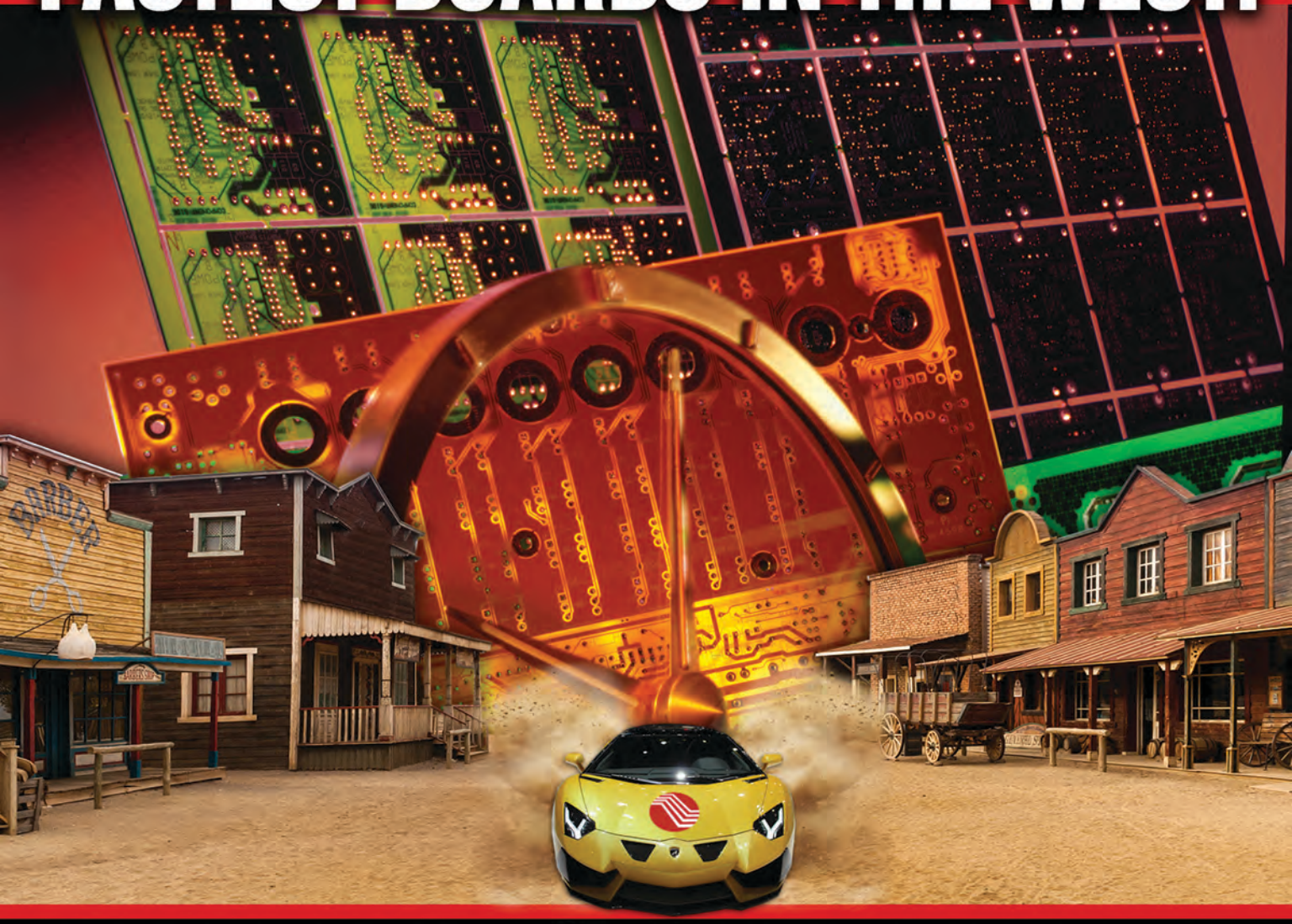

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DownStream: What a Long EDA Trip it's Been

No doubt about it: DownStream Technologies co-founder Joe Clark is an EDA veteran, with a history that dates back to the very beginning of EDA tools through the merger madness of the late '90s and beyond. I sat down with Joe during IPC APEX EXPO, and asked him about some of the changes he's seen, and the direction of DownStream as it enters its 15th year.

Andy Shaughnessy: *Joe, why don't you start off by giving everybody a real quick background about yourself and DownStream?*

Joe Clark: I actually began in EDA with a company called GenRad, or General Radio, which manufactured automatic test equipment (ATE) for verifying PCBs. The application there was mostly for functional testing. We created a PCB simulator to simulate the board and test if, for a given set of inputs, the outputs were correct. From that we ventured into simulation tools for custom components as custom ICs started to make an appearance in the market.

I went to work for Racal-Redac in the late '80s and early '90s before I moved to PADS Software, where I spent 10 years of my time. There we merged with Innoveda, which was formerly Viewlogic, and from there we spun out in 2002 to create DownStream Technologies.

Shaughnessy: *And 2002 was a great year to launch a start-up.*

Clark: That's a very good point. When I think about how long we've been doing DownStream it seems like it was only a couple of years ago, but it has been 15 years. When we spun out, it was really a bad time: The tech bubble had burst and then there was 9/11 and all the terrible things that surrounded that. It was just a bad time in general. Our view was the EDA industry up until then had focused primarily

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on what we called the upstream processes, like specifying the design, creating the schematic, the layout and so on, very few companies were focusing on the back end of the process, where we actually build things.

***Shaughnessy:** Where all the mistakes are.*

Clark: Exactly. Our belief was that in the whole process of NPI, new product introduction, it was equally important to focus on the front end, the upstream processes, as it was to focus on the back end, the manufacturing process – where we build things. Our vision for DownStream was to be the company that helps companies to bridge the gap or chasm between the "upstream" design processes and the "downstream" physical processes. This was an area of new product development that we believed would move from something that was "nice to do" to "mission critical".

Now, 15 years later, our vision was correct. Today, when you hear companies today talk about where they are focusing it is on the downstream processes. How do we improve that hand-off from design to manufacturing? A company's time for realizing a return on their products is always shrinking. The technology itself is always advancing, geometries continue to shrink, and flex circuits and embedded components are now a reality. The complexities have increased enough that is it no longer good enough to take the design and do the proverbial "hand it off over the wall."

Companies need to understand the manufacturing process and prepare the upstream processes to deal with them. Basically in a nutshell, where DownStream fits into the equation is we help companies bridge that gap, that chasm, between the upstream and downstream processes and how their products are built.

***Shaughnessy:** Right, designers like to design. They like doing the actual design, but they don't like doing the manufacturing prep part – for example, creating the documentation, and that's often where the mistakes are made. The people I have spoken to who use BluePrint say it pays for itself because they save time and effort, and reduce errors.*

Joe Clark

Clark: Yes, you're absolutely right. As a designer, you want to push the envelope with technology. That's fun and that's what is exciting. When it comes to doing the administrative portion of it and handing it off to the next phase, that's not so much fun, especially when the tools that you have had at your disposal historically are very difficult to use.

Our CAM350 product line is the defacto standard for verification and optimization of CAD files. CAM350 also has design rule checks to verify the Gerber layers match the design rules in your CAD system and your fabricator. Our design for fabrication tools ensure the board not only matches manufacturing capabilities, but also searches out design flaws that may affect manufacturing yields.

One of the things that's driving the success of our PCB documentation tool BluePrint is this concept of an intelligent design exchange format. Beginning with the groundbreaking concept of ODB++, which was a brilliant idea by Valor but is a proprietary format, we now have a true standard – the IPC-2581. Companies that want to improve new product introduction have realized great benefits from using a single data source. The acceptance of these intelligent formats we see as a shift in the design center of gravity from a proprietary CAD database which

you can't read or write to, to a neutral intelligent format where you can. Intelligent design formats such as the IPC-2581 can drive a company's internal and external processes, and the user has control over how much content they chose to include.

Now they can send off a single file to outside or captive manufacturing companies rather than having a bunch of disjointed files that have been produced from a proprietary format which aren't connected and which are difficult to be kept in-sync over the life of the product.

Another benefit of an industry standard design exchange format which often does not get mentioned is it enable new ideas, and gives companies choices for their EDA tools. It has been formats like IPC2581 that have enabled companies like DownStream Technologies to create and develop new ideas such as BluePrint to automate the documentation phase.

***Shaughnessy:** It's funny; most of the gains that we've seen lately have been in bridge tools from one tool to another, because that's where the problems are.*

Clark: It is where the problems are. The market, which we all have to pay attention to, is clearly saying "We want to do a better job of transitioning from that virtual space of design to the manufacturing space, whether it's a captive or an external contractor, which means we need to know more about the manufacturing process."

These intelligent design formats like IPC-2581 are enablers for that. We have the ability to take this intelligent format into our tools and then drive forward the downstream processes. These new ideas are good for the industry.

Companies with new ideas can actually participate, rather than in the past where we were circling the wagons and nobody could read or write the proprietary formats. The market doesn't want that any more. They want to be able to choose the tools that best fit their particular needs.

***Shaughnessy:** Do you think IPC-2581 is the way forward? Are all your tools going to be built around 2581?*

Clark: Yes, we do believe it is the way forward. And yes, we're committed to it. In fact, just before I met with you I was in one of the IPC committee meetings working on an amendment to Rev B of the IPC-2518 spec, and then we're going to begin defining what's going to come in Rev C. We need to deal with things like embedded components and flex. I think the biggest impact and trend that will be a game changer for all of us—upstream, downstream, wherever you are in the equation—is going to be from flex.

While we're committed to the 2581, that does not mean there aren't other formats out there that the market might require us to support, for example, ODB++ from Mentor and of course Gerber.

***Shaughnessy:** Aren't 90% of all designs still Gerber?*

Clark: Yes, this is true and may stay this way. When I go to a fabricator, I certainly can make an argument for the IPC-2581 which contains just the Gerber equivalent, and it's clear that there are huge benefits to sending off the Gerber equivalent if all they are sending is a single file to the fabricator, but there will still be companies that choose to go external with actual Gerbers; however, that's their choice and we support that. As much as it would make our automation easier, and our tools would fit better into everybody's processes and we could define the process, we can't force them to change; the market does that at its own pace. Our role is to listen and provide tools that support the varied processes that exist. At the same time we see ourselves as advocates to our customers and as such present new ideas and methodologies which we believe help our customers.

***Shaughnessy:** You can't be too picky, right? If people are using Gerber you've got to support that.*

Clark: Correct, but it doesn't exclude those same companies that might want to use Gerber externally from internally driving their processes with IPC-2581. Now they can choose tools that best fit their needs when the primary EDA vendor is not addressing their needs, i.e.,

for creating complex documentation. The traditional methods for creating PCB documentation that exist today just aren't cutting it any more. Companies are all coming to this conclusion as they look to improve their NPI and they turn to DownStream Technologies because we've got a robust PCB documentation tool. They're going to look at BluePrint to address their documentation needs, and today they can easily bring in such a tool because they can plug it into their process using the intelligent, neutral, design formats.

> "I believe that one of the key benefits is to the industry as a whole; if there's something we need in EDA, it's new ideas."

The IPC-2581 standard is multifaceted in terms of how it benefits the industry, the customers, and the OEMs. I believe that one of the key benefits is to the industry as a whole; if there's something we need in EDA, it's new ideas. By having this kind of format, it's enabling that kind of free thinking that maybe will allow new companies and new technologies to emerge.

***Shaughnessy:** What do you see down the road for DownStream?*

Clark: Well, our business is doing very well, and of course technology is constantly evolving. Couple this with companies now focusing on how to improve new product introduction, which must include and take into account manufacturing, and there's no shortage of opportunities for us. And as I said, embedded components and flex are going to be significant game changers. Companies have to deal with that from a design to manufacturing and documentation perspective so again, that represents opportunities for DownStream to offer solutions.

We're continually improving our product line. It's an interesting place where we fit into the new product development process. Because we are at the backend of the process we tend to be the set of tools that is used less frequently than the "upstream" tools such as schematic or PCB CAD.

One of the key things for us is to make sure our tools are easy to use and intuitive, because you have to pick it up, do the job, put it away and go on to the next design. You spend most of your time actually creating the design, and the goal is to ensure that the post-processing phase of NPI—where we execute our DFM checks and create our PCB documentation—is fast. The result of this is we are constantly looking for ways to improve the ease of use of the tools, and that keeps us busy. For example, we're currently in the process of re-doing our graphical user interface and adopting a more ribbon-like methodology.

The same is true for our CAM350 and DFMStream products. We're working with major companies to continue to refine and define the key DFM checks, the ones that really matter, and address the new ones that are coming all the time.

We're also constantly adding to our PCB documentation capability as well. A recent example of this is our assembly panel design tool. When a designer creates a schematic they are designing the circuitry, but at the end they'll have a picture which doubles as the document of the actual electrical circuit. Our assembly panel tool is analogous. One "designs" the assembly panel, and the end result is a picture which serves as the document. Our assembly panel tool is aimed at making it easy for the user, the PCB designer, to create exactly what the fabricator actually needs and will use to fabricate the users assembly panel, rather than the traditional tools which force the designer to function as a CAM engineer. Again, ease of use and the right tool for the specific task. And the task of creating assembly panels gets very complicated when you get into flip panels, and multi board panels where you have different PCBs in the same assembly panel.

***Shaughnessy:** It sounds like you'll have a plan to move forward.*

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Clark: We do indeed. The competition is tough today, but this forces us to try and be better. It's just like when we gambled in 2002 and created DownStream with this vision that there's going to be a requirement for better tools for transition from the virtual space to the physical space. Companies will have to verify their designs before they hand them off to manufacturing. They will need better tools to create their documentation. That gamble has paid off as our business results have shown now, 15 years on.

In addition, we're seeing other EDA vendors who are also offering tools like ours in their space. We have entered into a license and OEM agreement with Cadence, and they're packaging our tools into their offering to deal with the DFM and the documentation and the assembly panel design issues, because those are real issues that they're customers are demanding.

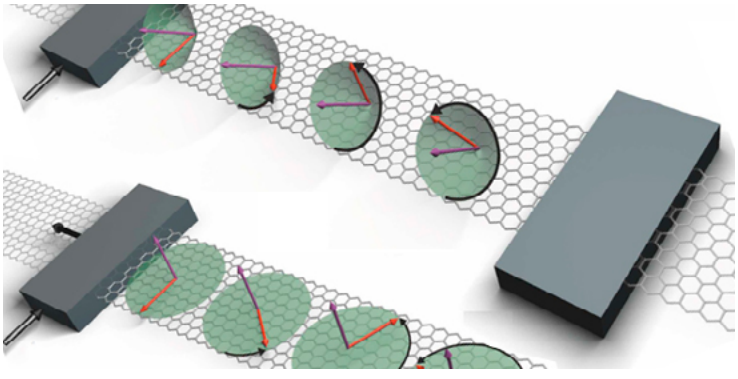
Shaughnessy: It's easier for them to do that than have to develop something new.

Clark: Absolutely. It's a very good relationship we have there, and we hope to have more relationships like that. The point in all that is when you start to see that your competition and companies that you complemented in the past are looking at your technology and offering similar capabilities, you know you're on the right track.

Shaughnessy: Joe, thanks so much for stopping by today.

Clark: Thank you, Andy. **PCBDESIGN**

Spin Lifetime Anisotropy of Graphene



One of the most fascinating puzzles for the graphene and spintronics communities is identifying the main microscopic process for spin relaxation in graphene. Conventional relaxation mechanisms have yielded contradictory results when applied to single-layer graphene. In an article published today in Nature Communications, researchers from the Institut Català de Nanociència i Nanotecnologia (ICN2) determine the spin lifetime anisotropy of spin-polarized carriers in graphene, which is expected to generate valuable information to overcome the above puzzle.

The present work demonstrates spin-lifetime anisotropy measurements in graphene and discusses them in light of current theoretical knowledge. The authors first determine the in-plane spin lifetime by conventional spin precession measurements with magnetic fields perpendicular to the graphene plane. Then, in order to evaluate the out-of-plane spin lifetime, they implement spin precession measurements under oblique magnetic fields that generate an out-of-plane spin population.

The results show that the spin lifetime anisotropy of graphene on silicon oxide is independent of carrier density and temperature down to 150°K, and much weaker than previously reported. Indeed, within the experimental uncertainty, the spin relaxation is isotropic. Together with the gate dependence of the spin lifetime, this indicates that the spin relaxation is driven by magnetic impurities or random spin-orbit or gauge fields.

The authors conclude that spin relaxation anisotropy measurements on specific substrates and with a controlled number of deposited adatoms will be crucial to increase the spin lifetime towards the theoretical limit and to find ways of controlling the spin lifetime. That is the path to ultimately develop unprecedented approaches for the emergence of spin-based information processing protocols relying on graphene.

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Romanian Electronics Industry Celebrates 25th Anniversary of TIE

by Joe Fjelstad
VERDANT ELECTRONICS

Professor Paul Svasta is with Politehnica University of Bucharest, Romania, Faculty of Electronics, Telecommunication and Information Technology and is head of the Center for Electronics Technology and Interconnection Techniques (CETTI). He is also a driving force for change and growth in Romania's small but vibrant electronics industry.

In 1989, Professor Svasta formulated a vision for Romania's future participation in the global electronics industry following the collapse of communism is his country. He surmised that it might be too late to catch the West and Asia in terms of production of hardware, but he knew that there would always be an increasing need for talented electronic product designers.

He thus set about the task of pulling together professors from other universities in Romania to cooperate in the development of opportunities for their students through a joint collaboration with industry in a forum where academicians, industry engineers and engineering students could teach and learn from each other and demonstrate their growing and improving capabilities. That forum they named TIE (Interconnection Techniques in Electronics) and late this April was held the 25th edition of the annual event.

The event included lectures from both universities and industry representatives of largely Romanian based companies from other EU nations and the US. The event included an informative panel discussion co-chaired by Professor

Figure 1: A team of evaluators review the work of the participants. Here, Alin Mazare of the Technical University of Pitesti and Cosmin Obreja of Continental Automotive Timisoara look over a student's work.

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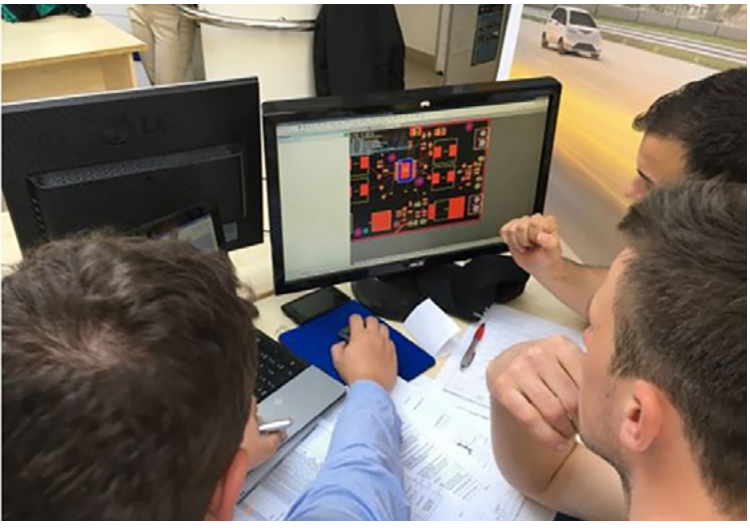

Figure 2: Each evaluation team is made up of members of academia and industry.

Figure 3: The winners of this year's competition: five honorable mentions and the third- and second-highest scoring designers.

Figure 4: Professor Paul Svasta congratulates the top scoring PCB designer, Voina Radu, of the Technical University of Cluj-Napoca.

Dan Pitica (Technical University of Cluj-Napoca), and Hartmut Hohaus (general manager of Miele Tehnica srl). The topic of discussion at this year's event was titled "Partnership in Practice" and underscored the importance of an ongoing partnership between university and industry and the many mutual benefits each receives from their interaction.

Many of the other technical presentations were focused on matters related to PCB design and it was fitting as the high point of the event was a competition among the students to design and layout a circuit for a specific product from a prospective bill of materials provided and meeting to the maximum extent possible a long list of design and product requirements. The students had just four hours to deliver a design which was then evaluated by a team comprised of a university instructor and a seasoned industry engineer against a checklist of specific design requirements.

The top performers are highly sought after and positions in an electronics company are virtually assured. Professor Svasta calls it "a win, win, win proposition, where the academia, supporting corporations and the students all benefit from the experience." Indeed, all parties do benefit, as the interactions allows the universities to keep current on what industry is seeking to better prepare their students, the industry gets talented and well-taught employees who can hit the ground running and the students get to confidence to know that they can perform to meet industry needs and secure a place in the PCB design workforce.

The entire conference was held in English, and all of those in attendance were highly proficient in English, which makes the program and its participant alumnae highly attractive to foreign companies. Some of the high-profile and familiar companies from the West who supported and participated this year

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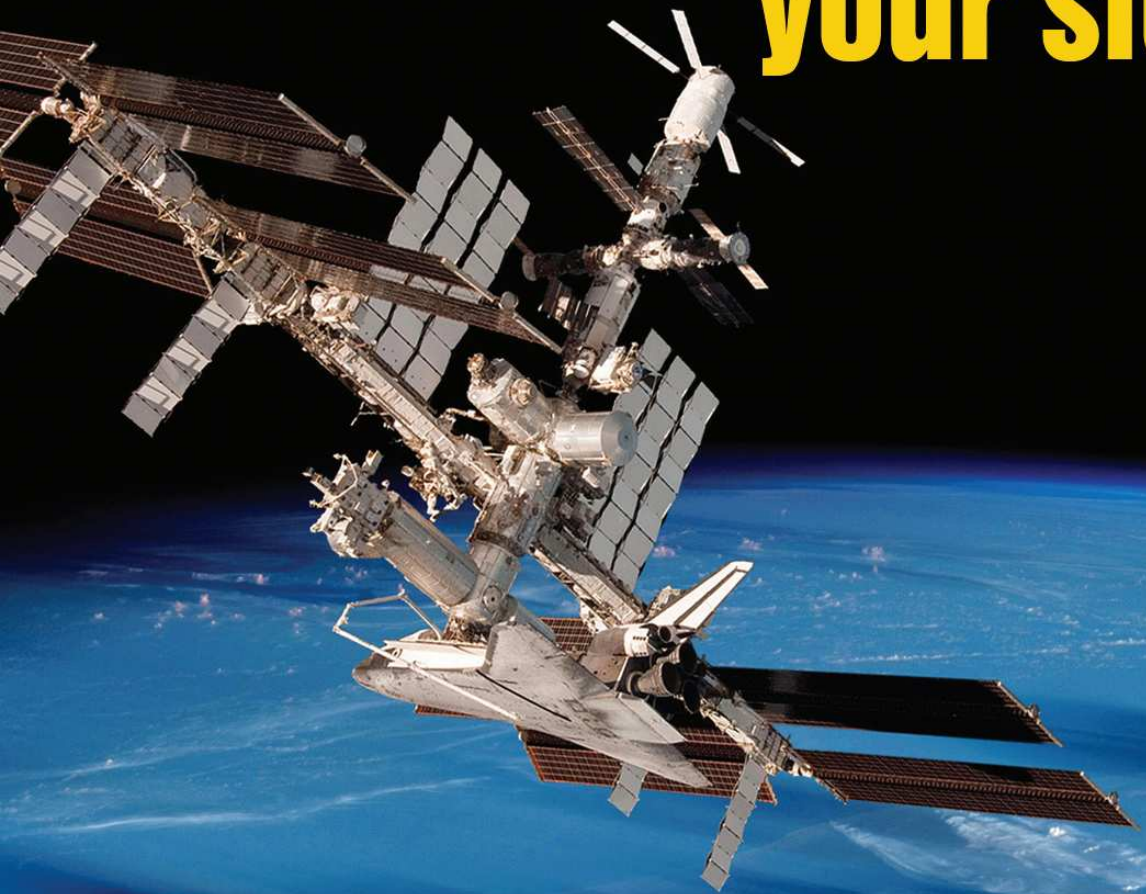

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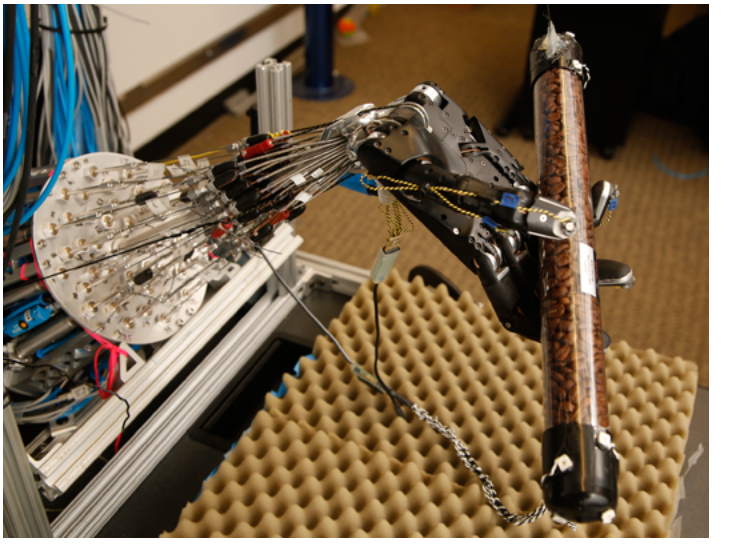
This year's conference brochure can be found here.

Next year's event will be held in April, 20-23, 2016 in Iasi, in the Northeastern part of Romania, and is eagerly looked forward to by all who were in attendance this year and likely by many others as word of the conference spreads beyond Romania's boarders. **PCBDESIGN**

Joseph (Joe) Fjelstad has more than 35 years of international experience in electronic interconnection and packaging technology in a variety of capacities from chemist to process engineer and from international consultant to CEO. He is the author of the fourth edition of Flexible Circuit Technology.

Five-fingered Robot Hand Learns to Get a Grip on Its Own



A University of Washington team of computer scientists and engineers has built a robot hand that can not only perform dexterous manipulation but also learn from its own experience without needing humans to direct it.

By contrast, the UW research team spent years custom building one of the most highly capable five-fingered robot hands in the world. Then they developed an accurate simulation model that enables a computer to analyze movements in real time. In their latest demonstration, they apply the model to the hardware and real-world tasks like rotating an elongated object.

With each attempt, the robot hand gets progressively more adept at spinning the tube, thanks to machine learning algorithms that help it model both the basic physics involved and plan which actions it should take to achieve the desired result.

Vikash Kumar, a UW computer science and engineering doctoral student, custom built this robot hand, which has 40 tendons, 24 joints and more than 130 sensors.

Building a dexterous, five-fingered robot hand poses challenges, both in design and control. The first involved building a mechanical hand with enough speed, strength responsiveness and flexibility to mimic basic behaviors of a human hand.

The UW's dexterous robot hand—which the team built at a cost of roughly $300,000—uses a Shadow Hand skeleton actuated with a custom pneumatic system and can move faster than a human hand. It is too expensive for routine commercial or industrial use, but it allows the researchers to push core technologies and test innovative control strategies.

The team first developed algorithms that allowed a computer to model highly complex five-fingered behaviors and plan movements to achieve different outcomes in simulation.

So far, the team has demonstrated local learning with the hardware system — which means the hand can continue to improve at a discrete task that involves manipulating the same object in roughly the same way. Next steps include beginning to demonstrate global learning — which means the hand could figure out how to manipulate an unfamiliar object or a new scenario it hasn't encountered before.

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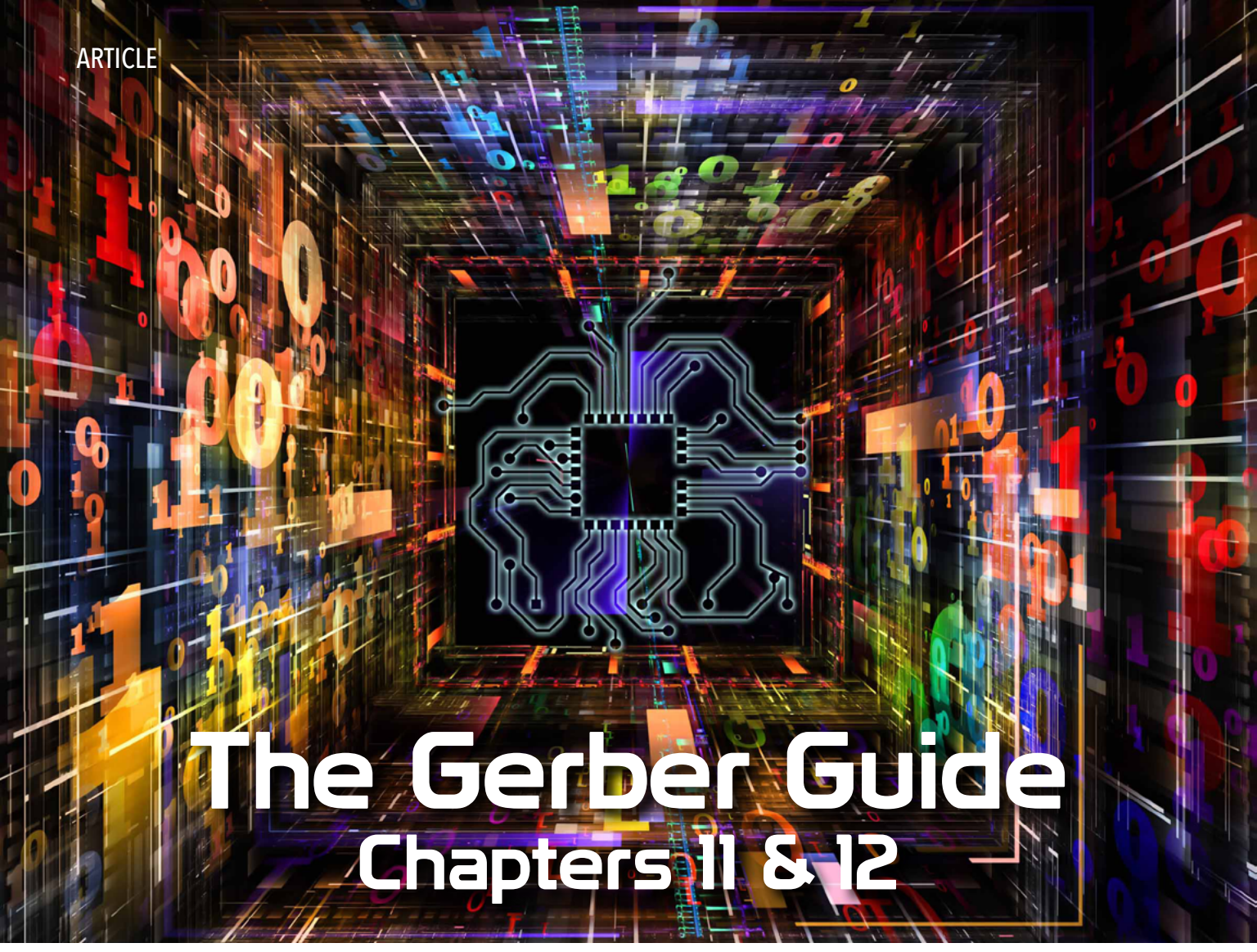


The Gerber Guide
Chapters 11 & 12

by Karel Tavernier
UCAMCO

It is possible to fabricate PCBs from the fabrication data sets currently being used; it's being done innumerable times every day, all over the globe. But is it being done in an efficient, reliable, automated and standardized manner? At this moment in time, the honest answer is no, because there is plenty of room for improvement in the way in which PCB fabrication data is currently transferred from design to fabrication.

This is not about the Gerber format, which is used for more than 90% of the world's PCB production.There are very rarely problems with Gerber files themselves; they allow images to be transferred without a hitch. In fact, the Gerber format is part of the solution, given that it is the most reliable option in this field. The problems actually lie in which images are transferred, how the format is used and, more often, in how it is not used.

Each month we look at a different aspect of the design to fabrication data transfer process. In this monthly column, Karel Tavernier explains in detail how to use the newly revised Gerber data format to communicate with your fabrication partners clearly and simply, using an unequivocal yet versatile language that enables you and them to get the very best out of your design data.

Chapter 11: Non-image Data

A PCB Fabrication set contains general PCB specifications such as thickness, finishes, ROHS compliance, etc., as well as commercial data: number ordered, addresses, delivery time.

There is currently no common standard governing this type of data. It is typically delivered as informal or formal data in plain text or in PDF files intended for human eyes.

PDF is a fine and widely supported format; however it is too complex for automatic data extraction. Remarkably enough, the best option for PCB fabrication data is a plain text format, as many fabricators have software that can automatically extract information from such files. Formal information is best expressed in structured text files: comma-separated values (CSV), XML, JSON or preferably YAML. YAML is well structured and human readable, and YAML files are the easiest and safest to automate.

Please do not use Excel, Word or PowerPoint formats. Firstly, by doing so you introduce yet more formats for your manufacturing partners to deal with. More importantly, they are not open formats: They are proprietary application formats whose specifications are rightfully closely-guarded secrets. They are not, therefore, data exchange formats, and their use adds unnecessary complications as automated data extraction is well-nigh impossible. They require dedicated interactive applications and cannot be built into automated workflows; what's more, version problems abound (e.g., between open source and Microsoft software). If you must choose between such formats and PDF, choose PDF without hesitation, but plain text files are best.

Often, general PCB data is delivered in drawings. This is an excellent and time-honored practice in all fabrication industries, but here too, data cannot realistically be extracted from drawings. Again, as automation protects against operator error, it is advisable to put all your general data in text files, even if it is already in a drawing.

Always place all of your general data in human-readable text files, informally or structured as in CSV, XML and YAML. Do not use Excel, Word or Power Point formats for this purpose.

Chapter 12: Number of Digits Used for Coordinates

Use the same resolution and number of digits (resolution) for all data layers. If you use different resolutions for different layers, the position of the different elements will be rounded differently. The result is that, say, via pads and drill pads end up being out of alignment. You can only hope then that the CAM engineer notices this and "snaps" the via pads to the drill holes. This of course changes the copper image, which is something the CAM engineer is not supposed to do, but he is also supposed to deliver a perfectly aligned PCB. So he's damned if he does, and he's damned if he doesn't.

Misalignment sometimes arises even when the same resolution is applied to all layers. This is usually because the output processors for Gerber and for Excellon round differently. As for other issues mentioned above, the simplest solution is to output the drill/rout layers in Gerber. (See Chapter 2 in this series.)

Ideally, Gerber files use six decimal places in inches and five or six decimal places in mm. If your software cannot produce these resolutions then get as close as you can. Some recommend the use of lower resolutions, probably to save a few bytes. Who cares about saving a few bytes? Don't follow this recommendation: lower resolution increases rounding errors. This not only affects alignment, but, more importantly, it increases the risk of serious problems because these rounding errors can make contours self-intersect, which is invalid and result in invalid arcs.

Low resolution is the root cause of most of the few image errors in Gerber files; it does not happen often but it makes no sense to take this risk to save a few bytes. Another reason given to use low resolution is that the drilling machine may not be able to handle big files. This may well be true but it is irrelevant: as we have already seen, the CAM system will output drill files exactly as the driller needs them.

Remember: Use the maximum precision for co-ordinates, and output all layers with the same precision. **PCBDESIGN**

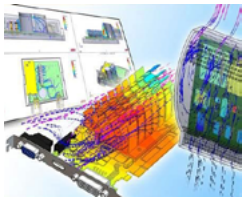
This column has been excerpted from the Guide to PCB Fabrication Data: Design to Fabrication Data Transfer.

Karel Tavernier is the managing director of Ucamco.

TOP TEN

Recent Highlights from PCBDesign007

1 Mentor Graphics Unveils PADS PCB Product Creation Platform



Mentor Graphics Corporation today announced a comprehensive product-creation platform based on PADS PCB software that enables individual engineers and small teams to solve the engineering challenges involved in creating today's electronic products. The PADS platform has been extended to enable engineers to develop PCB-based systems from concept through manufacturing hand-off.

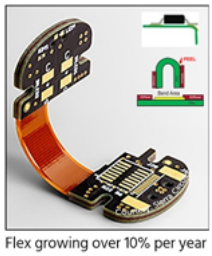
2 Brooks' Bits: How Many Vias Does It Take To…?

During 2015, Doug Brooks enjoyed a very productive collaboration with Dr. Johannes Adam, from Leimen, Germany. That collaboration resulted in several papers, but one in particular is relevant for this column, "Via Currents and Temperatures." In that paper, they used a simulation tool, thermal risk management (TRM), developed by Dr. Adam, to simulate current flowing through a via and then determine the temperature of the via. The results contradicted conventional wisdom.

3 Sunstone Circuits R&D: 3D Printing Great for Prototyping

We've been hearing a lot about 3D printing for the past few years. But where does 3D printing fit in with traditional rigid circuit board development? Sunstone Circuits recently completed a project that focused on that very question. Sunstone Product Manager Nolan Johnson explains why 3D printing is a viable option when it comes to jigs and parts of the support infrastructure that are needed when prototyping today's emerging technologies.

4 New Cadence Allegro Enhances Flex and Rigid-Flex Capabilities



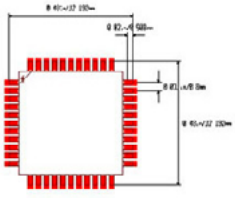
Flex growing over 10% per year

Cadence Design Systems has unveiled the Allegro 17.2-2016 portfolio, which enables a more predictable and shorter design cycle. The portfolio features comprehensive in-design inter-layer checking technology that minimizes design-check-redesign iterations and a new dynamic concurrent team design capability that accelerates product creation time by up to 50 percent.

5 Beyond Design: The Need for Speed—Strategies for Design Efficiency

Years of experience with one EDA tool obviously develops efficiency, whether the tool be high-end feature-packed or basic entry-level. However, there comes a time, with the fast development pace of technology, that one should really consider a change for the better to incorporate the latest methodologies. This month, Barry Olney will look at productivity issues that impede the PCB design process.

6 Accelerated Designs Adds Library Support for Zuken's CR-8000 and CR-5000



Zuken's CR-8000 and CR-5000PCB design platforms will now offer users access to more than 7 million symbols, footprints and 3D STEP models from Accelerated Designs. "We are looking forward to a successful partnership with Zuken supporting their CR-8000 and CR-5000 design platforms," says Frank Frank, CEO of Accelerated Designs.

7 Cadence Expands OrCAD to Address Flex and Rigid-Flex Challenges

Cadence Design Systems, Inc. announced the OrCAD 17.2-2016 release with new capabilities for OrCAD Capture, PSpice Designer and PCB Designer that address challenges with flex and rigid-flex design as well as mixed-signal simulation complexities in IoT, wearables and wireless mobile devices. This latest release reduces PCB development time by addressing the need to design reliable circuits for smaller, more compact devices.

8 Designers Notebook: Flexible and Rigid-Flex Circuit Design Principles, Part 5

The outline profile of the flexible circuit is seldom uniform. It may have portions that maintain a uniform profile, but one of the primary advantages of the flexible design is that the outline can be sculpted to fit into very oblique shapes. Vern Solberg explains.

9 Wild River: Simplifying SI so Engineers Can Focus on Design

Al Neves is founder and chief technologist of Wild River Technology, and he's a signal integrity engineer who likes to tell it like it is. So when I bumped into Al during DesignCon, I asked him to sit down for an interview. We discussed the paper he co-wrote for DesignCon and the challenges SI engineers are facing, as well as Wild River's efforts to take the black magic out of signal integrity.

10 DownStream's Fabstream.com and Electro-Labs.com Combine Resources to Launch Solo-Labs.com

Two leading online resources targeted to the electronic engineering professional and enthusiast combined resources today and launched Solo-Labs.com. The new resource brings together the assets of DownStream Technologies' DIY Maker initiative Fabstream.com and Electro-Labs.com to create a community-based portal where users can find electronic design tools, resources, project tutorials and knowledge to create PCB-based electronics.

PCBDesign007.com for the latest circuit design news and information—anywhere, anytime.

Events

For IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out The PCB Design Magazine's event calendar.

IPC Reliability Forum
May 17-19, 2016
Dusseldorf, Germany

IPC Regulatory Compliance Update-ROHS, REACH, Conflict Minerals
May 19, 2016
Dusseldorf, Germany

iNEMI 2017 Roadmap North American Workshop
May 31, 2016
Las Vegas, NV, USA

JPCA Show 2016
June 1–3, 2016
Tokyo Big Sight
Tokyo, Japan

IPCA EXPO 2016
August 18–20, 2016
Delhi, India

IPC India / electronica India 2016 / productronica India 2016
September 21–23, 2016
Bengaluru, India

IPC Fall Meetings
September 24–30, 2016
Rosemont, Illinois, USA

SMTA International 2016
September 25–29, 2016
Rosemont, Illinois, USA

electronicAsia
October 13–16, 2016
Hong Kong

TPCA Show 2016
October 26–28, 2016
Taipei Nangang Exhibition Center
Taipei, Taiwan

Electronica
November 8–11, 2016
Munich, Germany

International Printed Circuit & Apex South China Fair (HKPCA)
December 7–9, 2016
Shenzhen, China

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