PCB007 PRESENTS



June 2015

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# Flexible, Stretchable and Wearable

## A High-Reliability, Stress-free Copper Deposit for FPC, Polyimide and Rigid-Flex

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## June Featured Content

### FLEXIBLE, STRETCHABLE & WEARABLE

This month, a comprehensive view of the scope of flex circuit technology is presented in features from OM Group, Multek, DuPont, ESI, and more.

*Cover photo courtesy of MC10, www.mc10inc.com*











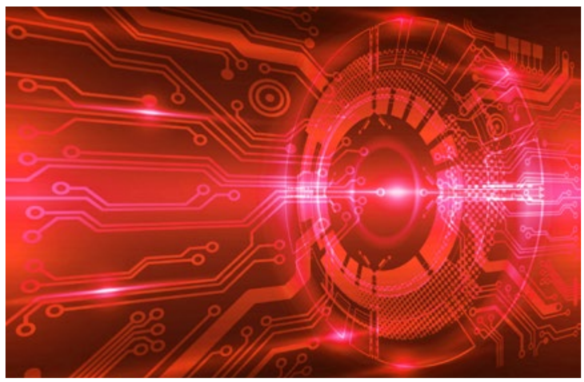



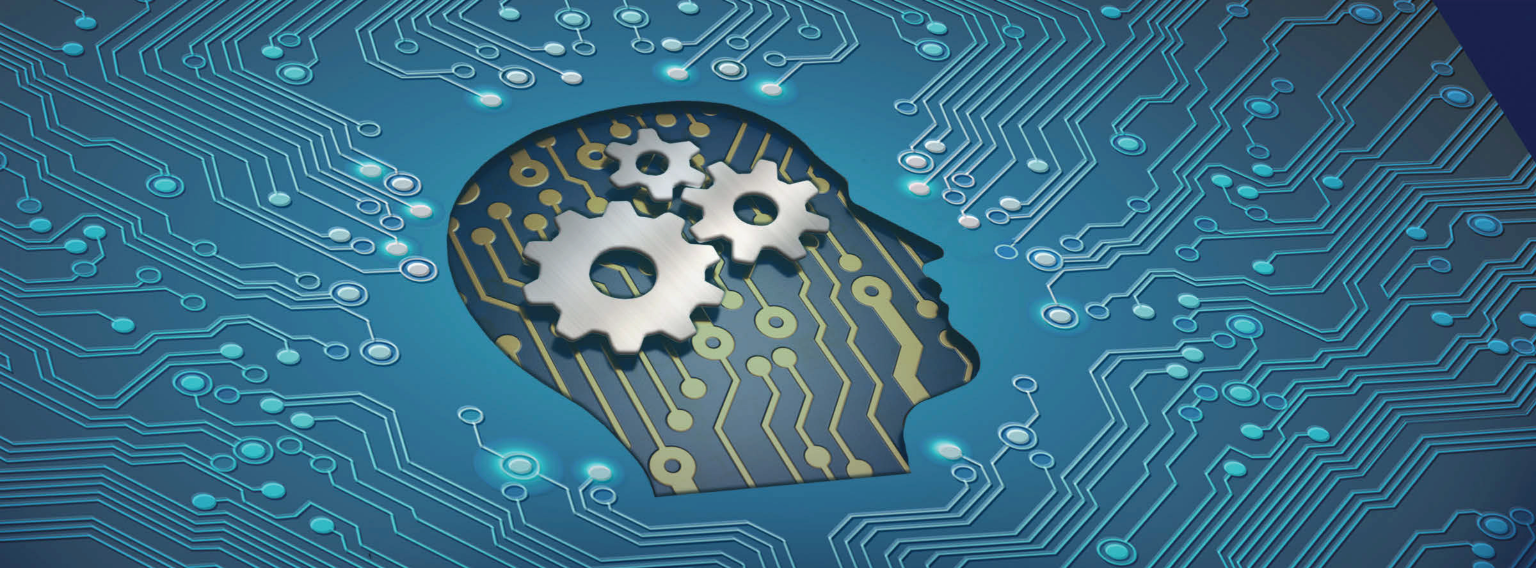

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PATTY'S PERSPECTIVE

# Flexible, Stretchable, and Wearable: If You Can Dream it, You Can Create it!

**by Patty Goldman**
I-CONNECT007


It seems that flex circuit technology is definitely coming into its own. The market for flex circuitry has always been growing, but now it is rapidly accelerating, with new technologies and new applications in the news nearly every day. Flex is not just in your laptop and camera anymore, it is in your car, in space, and on your body. In other words, flex is everywhere.

We originally intended this issue to be centered on flexible circuits, but it quickly became apparent that we needed to broaden the scope and include all (well, at least some) of the new and exciting things going on these days in the world of flexible everything. As such, we have garnered a trove of authors, with much information to impart on the above-mentioned.

Our cover story from OM Group discusses the processing of flex materials using a stress-free plating technology for both flex and rigid-flex materials.

Then, Dr. Joan Vrtis of Multek gives a great market overview of that relatively new industry most often called 'wearables.' She points out that wearables are not new, but when combined with electronics, this industry is only limited by the imagination, as the technology to make it happen is rapidly evolving.

Looking at another flex industry segment (flex segmented!), Maarten Cauwe and co-authors from imec pull our interest in a different direction as they explore two technologies for flexible and stretchable circuits in space applications.

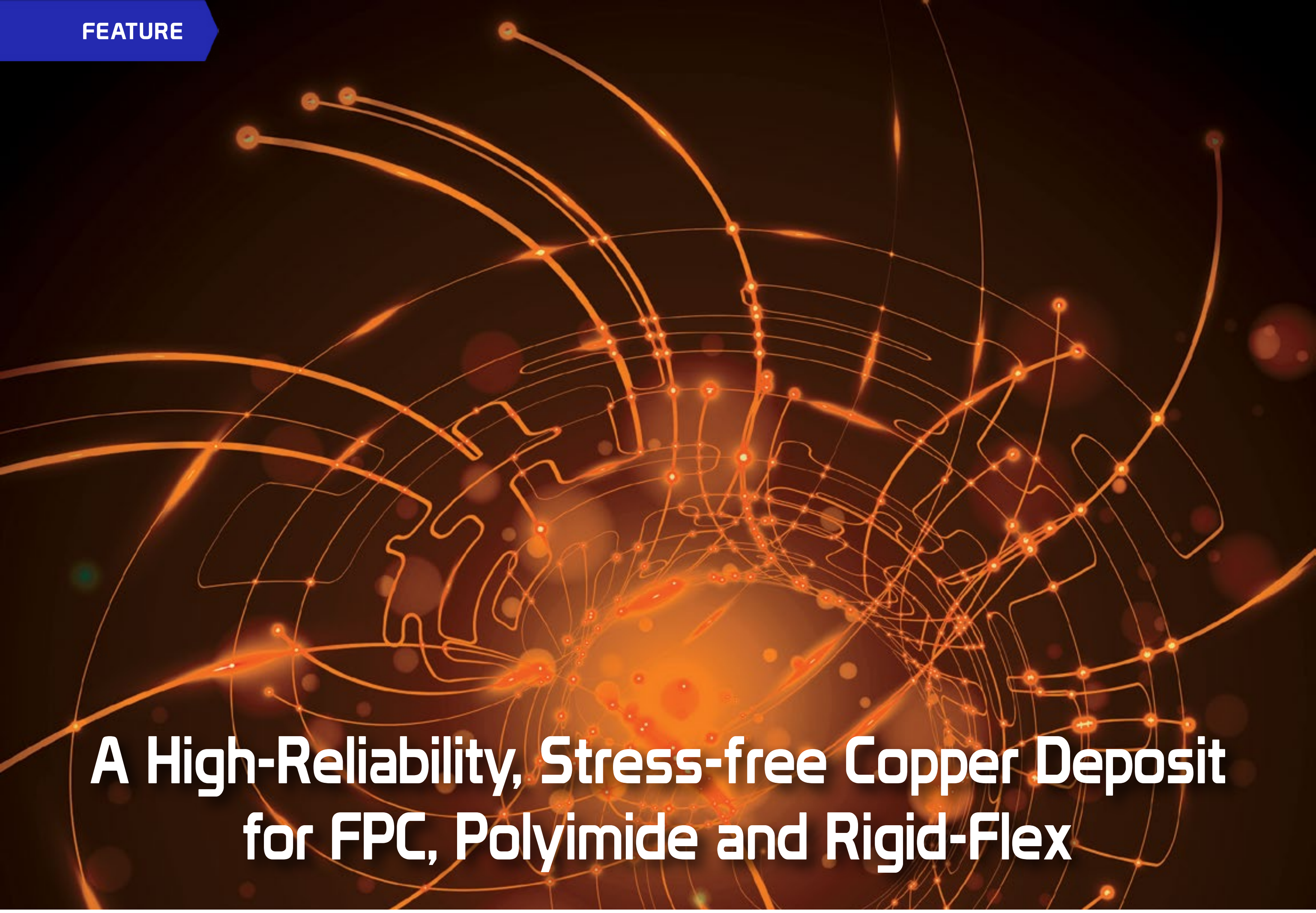
So back to the beginning: Two articles discuss new materials to help make some of this happen. Panasonic's Yoshioka et al., present a high-performance substrate for stretchable electronics, while Dupont's Sidney Cox discusses a new flex material for high-temperature applications.

Also on the topic of the processing of flex materials, Patrick Riechel of ESI reviews three technologies for microvia drilling and cutting. Rounding out the processing topic is columnist Todd Kolmodin with a brief overview on testing flex circuits.

This month is a perfect time to introduce our two newest columnists, who will become regular contributors to our Flex007 Weekly Newsletter that publishes every Thursday. As her first subject, Tara Dunn of Omni PCB chose "Flex-to-Fit"—another flex industry subset that is only limited by the imagination. And last but not least, Dave Becker of All Flex presents his summary of wearable technology.

There's a lot going on in flexible, stretchable, wearable technology and there is much to learn! **PCB**

Patricia Goldman has been in the PCB industry for 30+ years, working in areas that include, R&D of imaging technologies, wet process engineering, and sales and marketing of PWB chemistry, photoresist and glass reinforcements. Goldman has chaired several IPC committees and subcommittees and also served as TAEC chairman. Her new column, Patty's Perspective, will be appearing here monthly. To contact Goldman, click here.



# A High-Reliability, Stress-free Copper Deposit for FPC, Polyimide and Rigid-Flex

**by Jason Carver and Alvin Kucera**
OM GROUP ELECTRONIC CHEMICALS

**Abstract**

Today's wide variety of laminate materials and specialized dielectric choices pose a challenge for process engineering. In particular, smooth surfaces, such as polyimide, flex circuit substrates and rigid-flex constructions with window cut-outs, can be a challenge for electroless copper and plating processes. Conventional electroless copper systems often required pretreatments with hazardous chemicals or have a small process window to achieve a uniform coverage without blistering. To overcome the challenge of metallizing smooth surfaces, a new stress-free electroless copper was developed to serve this important sector of the printed circuit industry.

**Introduction**

As the thermal, physical, chemical and electrical properties of PCBs have advanced, so too have the substrates of construction. With a wide variety of substrates available, it is becoming increasingly difficult to accommodate these new substrates in current manufacturing processes[1]. Polyimide resins (PI), for example, provide exceptional thermal and chemical stability but remain challenging with industry standard processes. In particular, electroless copper deposition, the most commonly used method of metallizing a nonconductive substrate, is susceptible to blistering or peeling due to the low adhesion of the copper film to the substrate. Typically, electroless copper films require mechanical anchoring to provide adhesion to a substrate to prevent blistering. A roughened surface is commonly created with a chemical or plasma etch process to help create anchoring sites. Conventional chemical etches, which were primarily designed for epoxy substrates, are generally ineffective at activating PI substrates[2]. Plasma etching, which is effective at etching PI, is still insufficient to prevent peeling and blistering[3]. Some manufacturing processes have resorted to using an alkaline solu-

tion containing hydrazine[4]. While this can be effective at improving adhesion of electroless copper films, hydrazine is extremely hazardous and challenging to handle safely. In addition, many material types, such as those that contain adhesive bonding layers, are incompatible with strong alkaline solutions.

Due to the fact that most surface treatments are ineffective, or not practical or compatible in some situations, it is critical that the electroless copper process provides a significantly wide processing window to alleviate blistering defects and accommodate a variety of substrate types. The most common commercially available electroless copper plating solutions are not designed to meet these requirements. It is known that blistering and peeling of the copper deposit is also a function of the internal stress and strain of the deposit and that additives can be included in an electroless copper solution that affect the properties of the resulting electroless copper deposits (5–7). However, inclusion of additives may affect PCB reliability and careful selection is necessary. In this study, we evaluate select additives in an electroless copper system for their influence on the deposit stress and, ultimately, their effect on the reliability of a PCB by thermal shock and interconnect stress test (IST).

## Experimental

Electroless copper plating solutions comprised of 0.03 M copper sulfate, 0.15 M formaldehyde, 0.08 M metal chelator, 0.1-0.3 M sodium hydroxide and select stress reducing additives were used for electroless copper metallization. The substrates were activated with palladium prior to electroless copper metallization. One to 2 microns of electroless copper was deposited onto the substrates of interest. Substrate was also processed through the aforementioned solution to increase chemical byproducts of the electroless copper reaction, represented by an increase in specific gravity, from a specific gravity of 1.03 to 1.10. These solutions were evaluated at various points within this range. PI substrates were used for blister evaluation.

Internal stress was evaluated using a Yamamoto JIS-H8626 spiral contractometer with a 0.15 mm nickel and teflon coated spiral per ASTM B 636-84 (2001).

A 1.57 mm thick interconnect defect (ICD) solder shock coupon comprised of 8 layers of alternating 1 oz. and ½ oz. copper and 1.02 mm plated through holes (PTH) was used for evaluation. Substrate of construction was an epoxy FR-4 with a 180°C glass transition temperature ($T_g$). after electroless copper metallization these coupons were electroplated in a commercially available sulfuric acid based copper plating solution to increase the total copper deposit thickness to 28–30 microns prior to ten thermal shocks at 288°C for 10 seconds each in accordance with IPC-TM-650 2.4.13f. cross sectional evaluation was performed on seven PTHs per coupon.

Reliability was also evaluated using an IST testing system from PWB Interconnect Solutions Inc. (Ottawa, ON CA). IST coupon design GM40001A with a thickness of 3.18 mm comprised of 14 ½ oz. copper layers was used for evaluation. The coupon was constructed using

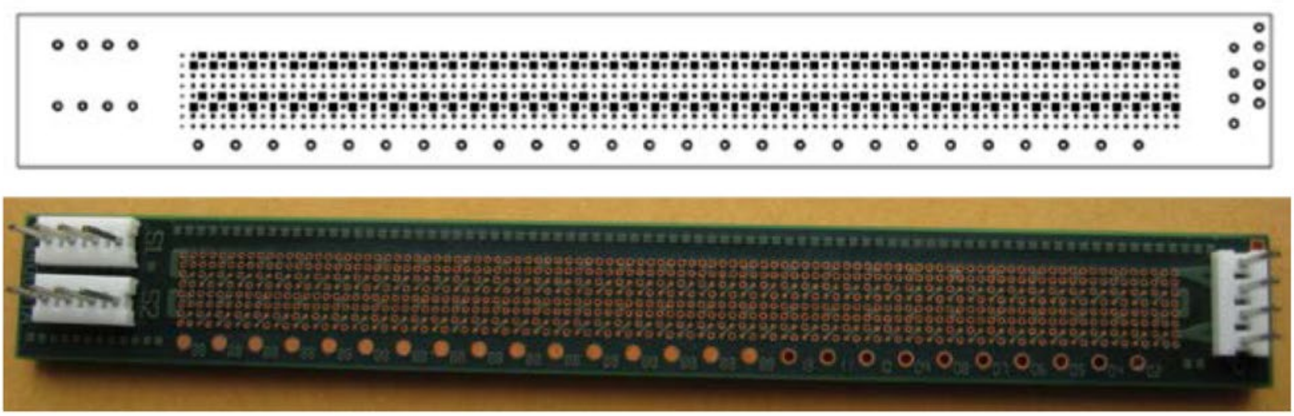


Figure 1: IST GM40001A.

the same substrate as the ICD coupon and contained 0.25 mm and 0.38 mm PTHs and 0.15 mm micro vias (MV). All coupons were precycled at 260°C six times to simulate the assembly process. The IST equipment was set to cycle between 25°C and 150°C (PTH) or 25°C to 190°C (MV) with three minutes of heating and two minutes of cooling. Coupons were tested for 1000 cycles or to failure defined as a 10% increase in resistance. Failure mode was evaluated and documented. This coupon is comprised of two circuits, S1 being PTH and S2 being MV, with S1 being evaluated first followed by S2. These IST coupons were electroplated in a commercially available sulfuric acid based copper plating solution to increase the total copper deposit thickness to 28–30 microns. A picture of the IST coupon is shown in Figure 1.

### Results and Discussion

The effect of the additives on the electroless copper deposit was first evaluated using PI substrates that historically have been problematic for electroless copper processing. These materials are all PI substrates found commonly in the manufacturing of flexible PCBs. Comparative studies were visually performed with and without the additives to determine their effectiveness at reducing or eliminating blistering and peeling of the copper deposit. Figures 2 and 3

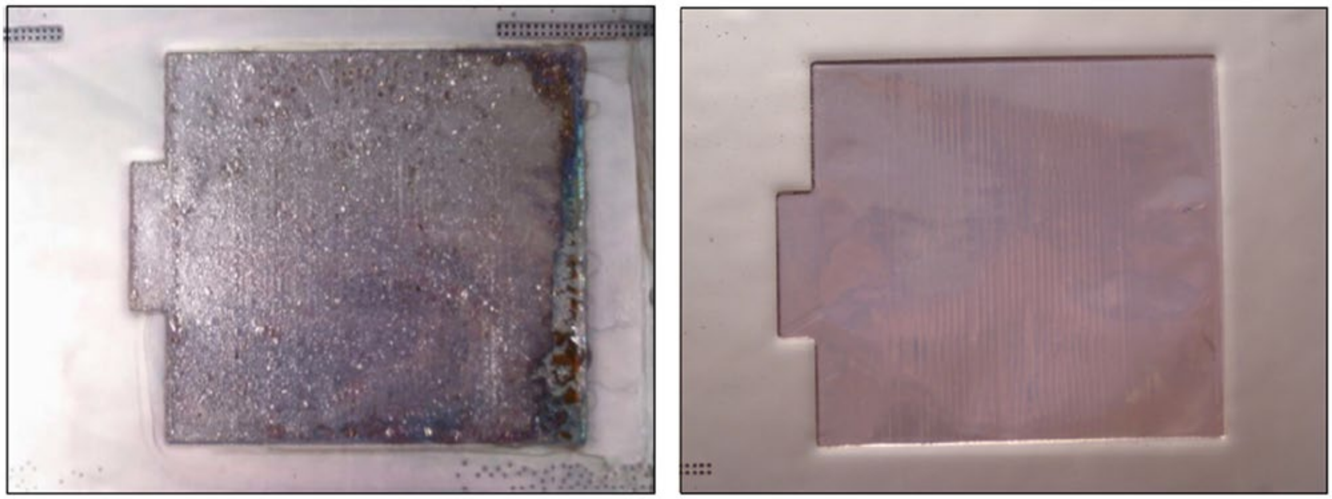


Figure 2: Sequentially laminated rigid-flex PI window cut-outs exposed to electroless copper processing. Electroless copper (left) and electroless copper with stress reducing additives (right).

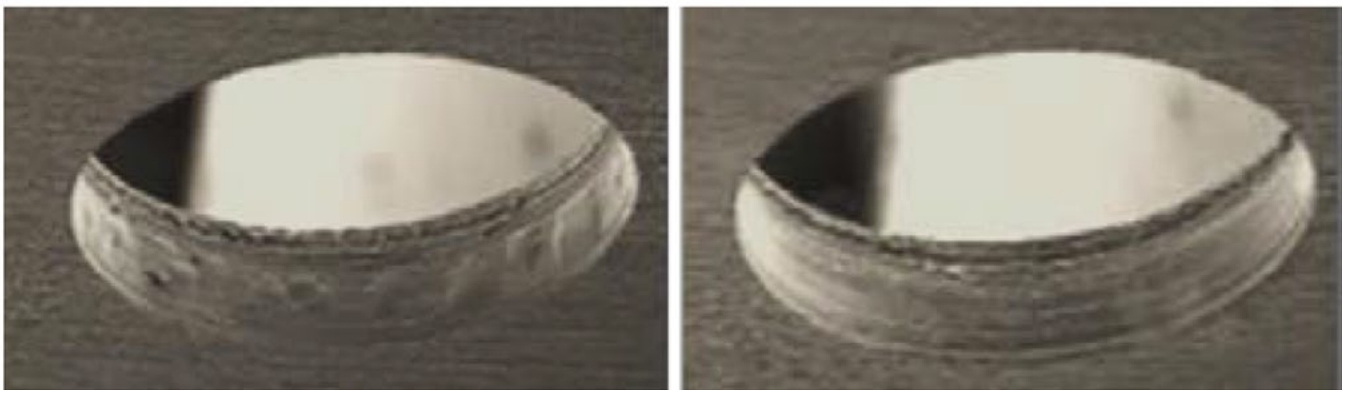


Figure 3: Flexible PI PTH. Electroless copper (left) and electroless copper with stress reducing additives (right).

represent materials that have shown poor coverage on an additive free electroless copper solution. With the addition of the additives a significant improvement is observed.

The reduction of blistering is attributed to reduced internal stress of the copper deposit. Additives included in the electroless copper solution effect the stress of the resulting electroless copper deposit. Electroless copper deposits normally exhibit compressive stress and tend to lift, or blister, off of smooth surfaces that lack mechanical anchoring sites. With the proper selection of additives the stress of the deposit can be significantly reduced.

Deposit stress can be measured in a number of ways. A common method in the electroplating industry is through the use of a spiral contractometer. The copper deposits of four electroless copper solutions containing different additives were evaluated using a Yamamoto JIS-H8626. Figure 4 indicates that internal stress of the deposit is significantly affected by additives. Typical electroless copper solutions utilized in PCB manufacturing are similar to Electroless B and C and D. With the addition of select stress reducing additives, labeled Electroless A, the stress of the deposit is reduced significantly.

Electroless copper solutions containing additives from Electroless A in Figure 4 were evaluated further to determine the influence on PCB reliability. Specifically, the resulting copper deposit's reliability was evaluated on interconnects within multilayer PCBs when exposed to thermal stress. Substrate was processed through these solutions and replenished accordingly with chemical components to maintain consistent operating conditions. Operating in this way allows the solution to increase in electroless copper byproducts, such as formate, sulfate, additives, etc., similar to how commercial electroless copper systems are operated. In general, electroless copper solutions are controlled by analysis of the main chemical components as well as the specific gravity of the solution. As electroless copper solutions increase in specific gravity, undesired properties, such as solution instability, deposit defects, and byproduct formation, become more pronounced. Ultimately,

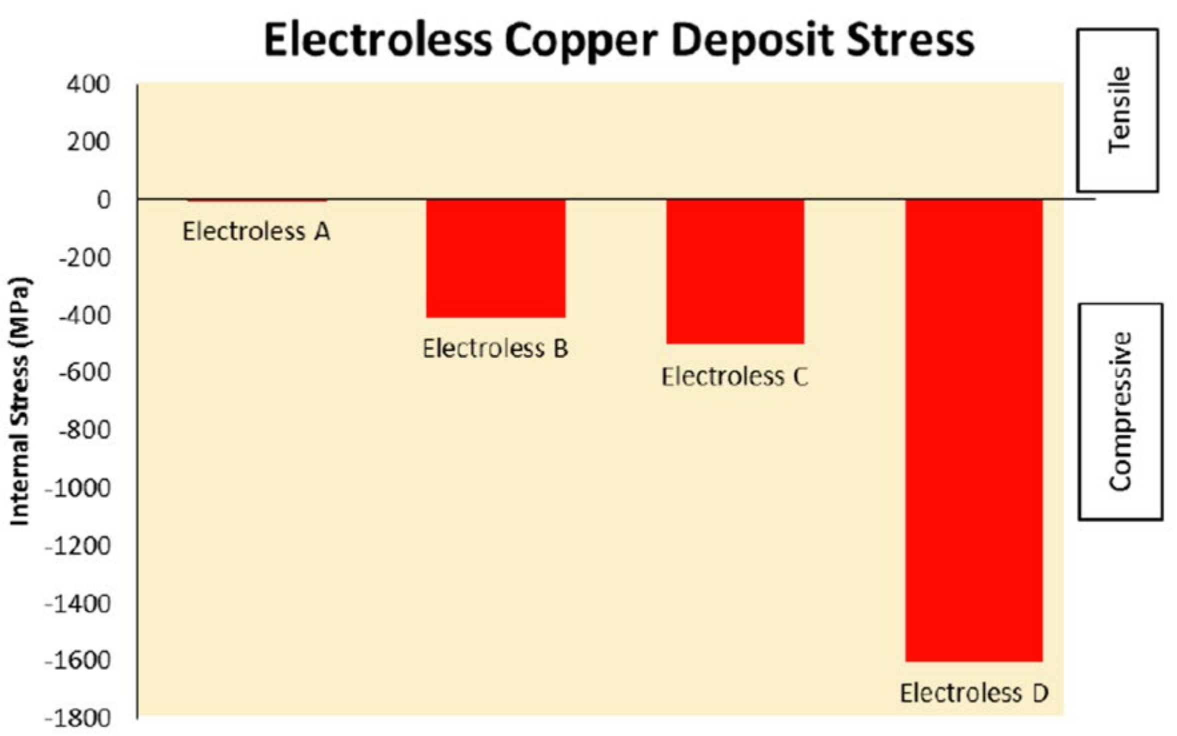



Figure 4: Electroless copper deposit stresses measured by spiral contractometer. Additives in the electroless copper solution have a significant influence on the resulting deposit stress.

these properties can affect the reliability of the copper deposit.

ICD solder shock test coupons were processed through these solutions at various specific gravity levels and evaluated accordingly. In all situations there were no ICDs encountered. Each data point in Figure 5 represents 12 interconnects evaluated in seven PTHs for a total of 84 opportunities per data point. In total, approximately 4500 interconnects were evaluated.

IST coupons were also evaluated after processing through the electroless copper solutions with stress reducing additives. Table 1 shows the results of each test according to specific gravity and deposit thickness. Test coupon outcomes are reported as cycles to failure and results listed as power, sense or accept. Coupons that reached 1000 cycles received an accept result. Failure before 1000 cycles was initially determined by the IST system to be on the power or sense circuit. In general, a failure in the power circuit can indicate a failure at the copper barrel/interlayer interface which is of primary interest when evaluating an electroless copper deposit interconnect reliability. A failure in the sense circuit is typically attributed to a failure in the PTH copper plating (i.e., a barrel crack). However, in both cases cross section evaluation is necessary to confirm failure mode.

As mentioned previously, all IST coupons that failed to reach 1000 cycles were evaluated by cross section to determine the root cause of failure. In all instances, the failure was attributed to cracking of the copper plating, or barrel cracks, as shown in Figure 6. There were no failures attributable to the electroless copper deposit or ICDs.

Next, life data regression analysis was performed with the two predictors, specific gravity and deposit thickness, to determine their effect on IST cycles to failure. The data was fit using a Weibull distribution. In both cases, the two factors were not statistically significant at $\alpha = 0.05$. Since the two factors were not significant, the results were pooled together and fitted to a Weibull distribution shown in Figure 7. The results were then compared to historical data of electroless copper without stress reducing ad-

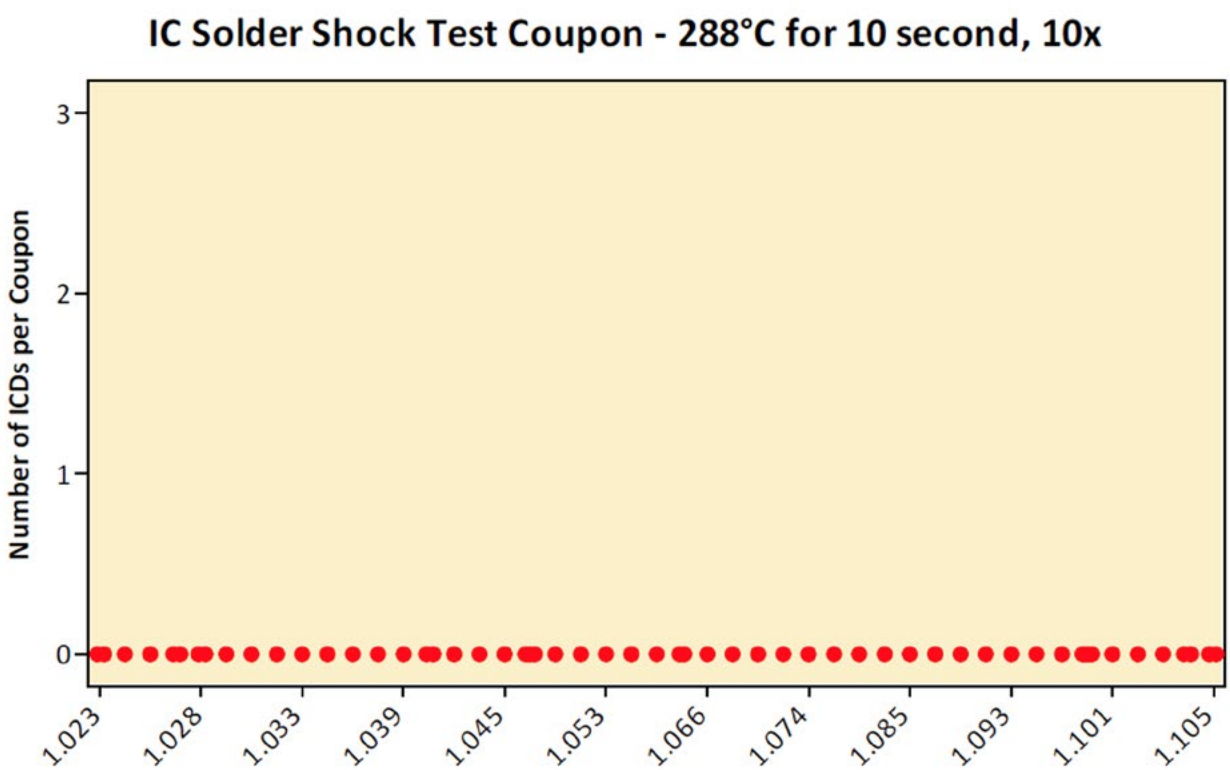



Figure 5: 10x solder shock test from a bath specific gravity of 1.02–1.10.

| Specific Gravity | Electroless Copper Deposit Thickness (µm) | S1 Result | S1 Cycles | S2 Result | S2 Cycles |
|---|---|---|---|---|---|
| 1.06 | 1.55 | Sense | 880 | Accept | 1000 |
| 1.06 | 1.55 | Accept | 1000 | Accept | 1000 |
| 1.06 | 1.55 | Accept | 1000 | Accept | 1000 |
| 1.06 | 1.55 | Accept | 1000 | Accept | 1000 |
| 1.06 | 1.55 | Accept | 1000 | Accept | 1000 |
| 1.09 | 2.03 | Accept | 1000 | Accept | 1000 |
| 1.09 | 2.03 | Sense | 985 | Accept | 1000 |
| 1.09 | 2.03 | Accept | 1000 | Accept | 1000 |
| 1.09 | 2.03 | Accept | 1000 | Accept | 1000 |
| 1.09 | 2.03 | Accept | 1000 | Accept | 1000 |
| 1.04 | 1.5 | Sense | 486 | Accept | 1000 |
| 1.04 | 1.5 | Accept | 1000 | Accept | 1000 |
| 1.04 | 1.5 | Sense | 586 | Accept | 1000 |
| 1.04 | 1.5 | Accept | 1000 | Accept | 1000 |
| 1.04 | 1.5 | Accept | 1000 | Accept | 1000 |
| 1.04 | 1.5 | Accept | 1000 | Accept | 1000 |
| 1.092 | 1.73 | Accept | 1000 | Accept | 1000 |
| 1.092 | 1.73 | Accept | 1000 | Accept | 1000 |
| 1.092 | 1.73 | Sense | 768 | Accept | 1000 |
| 1.092 | 1.73 | Sense | 999 | Accept | 1000 |
| 1.092 | 1.73 | Sense | 649 | Accept | 1000 |
| 1.07 | 1.23 | Sense | 966 | Accept | 1000 |
| 1.07 | 1.23 | Accept | 1000 | Accept | 1000 |
| 1.07 | 1.23 | Accept | 1000 | Accept | 1000 |

| Specific Gravity | Electroless Copper Deposit Thickness (µm) | S1 Result | S1 Cycles | S2 Result | S2 Cycles |
|---|---|---|---|---|---|
| 1.07 | 1.23 | Sense | 653 | Accept | 1000 |
| 1.07 | 1.23 | Sense | 864 | Accept | 1000 |
| 1.07 | 1.23 | Sense | 938 | Accept | 1000 |
| 1.1 | 1.32 | Accept | 1000 | Accept | 1000 |
| 1.1 | 1.32 | Accept | 1000 | Accept | 1000 |
| 1.1 | 1.32 | Accept | 1000 | Accept | 1000 |
| 1.1 | 1.32 | Accept | 1000 | Accept | 1000 |
| 1.1 | 1.32 | Accept | 1000 | Accept | 1000 |
| 1.07 | 1.18 | Accept | 1000 | Accept | 1000 |
| 1.07 | 1.18 | Accept | 1000 | Accept | 1000 |
| 1.07 | 1.18 | Accept | 1000 | Accept | 1000 |
| 1.07 | 1.18 | Accept | 1000 | Accept | 1000 |
| 1.07 | 1.18 | Accept | 1000 | Accept | 1000 |
| 1.075 | 0.94 | Accept | 1000 | Accept | 1000 |
| 1.075 | 0.94 | Accept | 1000 | Accept | 1000 |
| 1.075 | 0.94 | Accept | 1000 | Accept | 1000 |
| 1.075 | 0.94 | Accept | 1000 | Accept | 1000 |
| 1.075 | 0.94 | Accept | 1000 | Accept | 1000 |
| 1.075 | 0.94 | Accept | 1000 | Accept | 1000 |
| 1.1 | 1.14 | Accept | 1000 | Accept | 1000 |
| 1.1 | 1.14 | Accept | 1000 | Accept | 1000 |
| 1.1 | 1.14 | Accept | 1000 | Accept | 1000 |
| 1.1 | 1.14 | Accept | 1000 | Accept | 1000 |
| 1.1 | 1.14 | Accept | 1000 | Accept | 1000 |

Table 1. IST GM40001A Results.

Figure 6: Examples of IST sense circuit failures identified by cross section evaluation as copper plating cracks.

ditives and similar coupon construction. The comparison is shown in Figure 8. Note that the historical IST data was performed at a lower preconditioning temperature of 230°C. It is generally accepted that preconditioning at higher temperatures is a more critical test with regard to IST failure.

The additives had no negative effects on interconnect reliability of the electroless copper deposit when compared to historical data of an

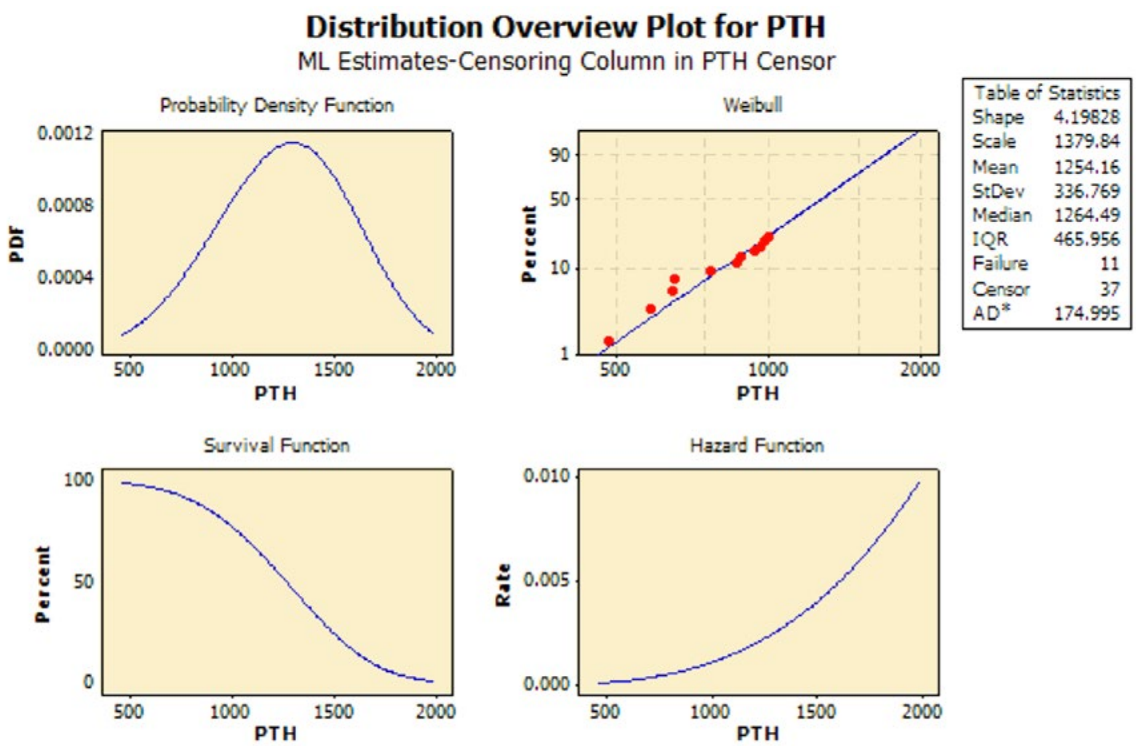



Figure 7: Distribution overview plot of all IST coupons based on cycles to failure. The data was right censored at 1000 cycles.

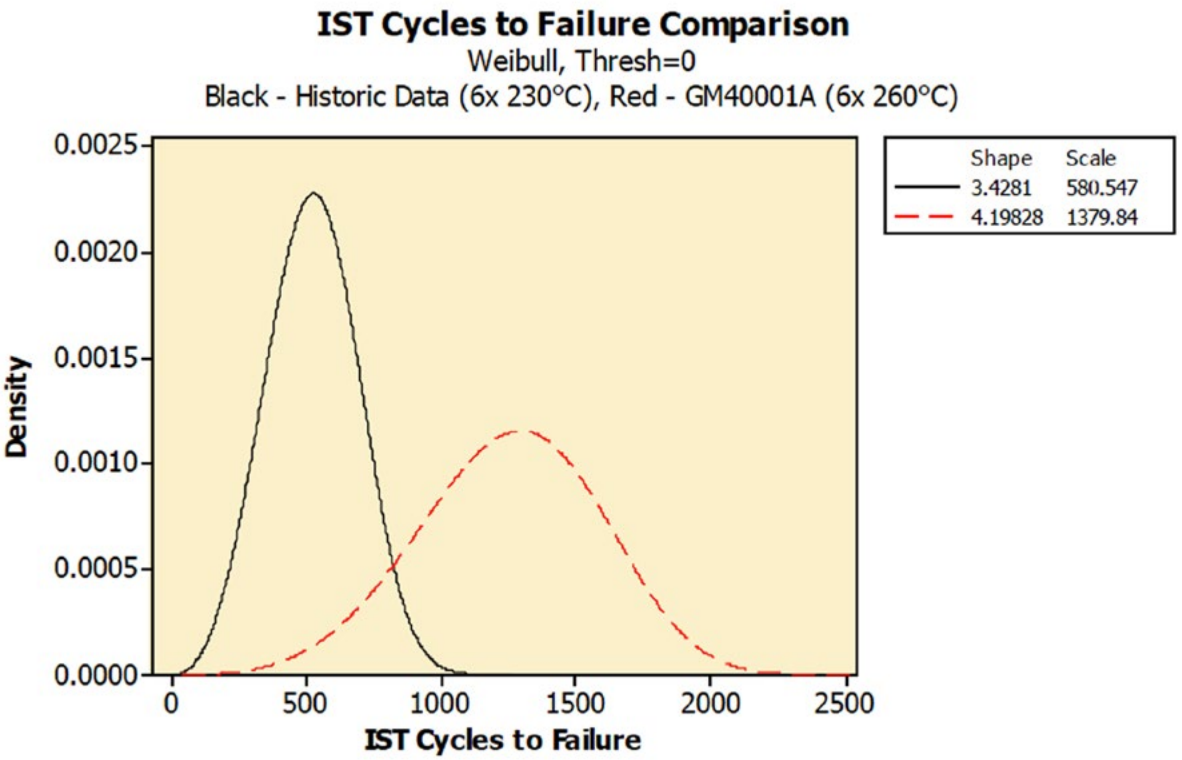



Figure 8: Comparison of IST cycles to failure of the PTH with (red) and without (black) stress reducing additives.

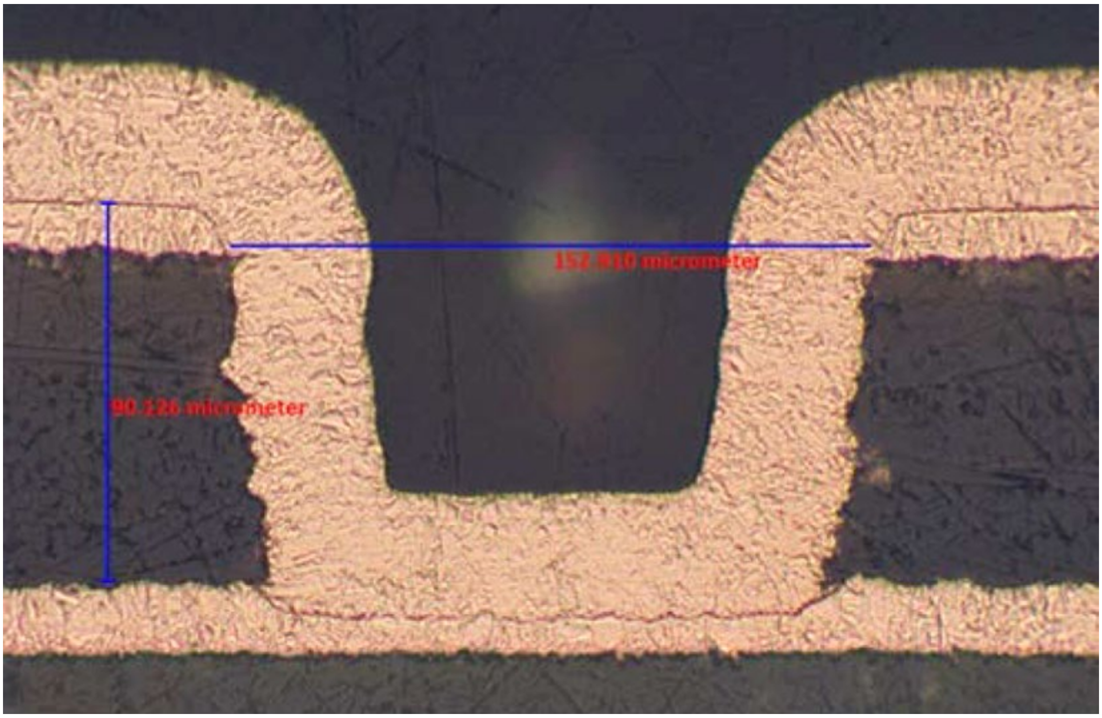



Figure 9: Cross-section of an IST coupon MV after 1000 cycles.

electroless copper solution without stress reducing additives. Next, the S2 circuit, which contained the MVs, was evaluated. After 1000 cycles there were no defects present at any parameters evaluated. A cross section is shown in Figure 9. No additional evaluation was necessary. Due to the IST coupon design and test parameters used in this study, the S2 circuit has already experience up to 1000 cycles during testing of the S1 circuit. Therefore, the S2 circuits have experienced up to 2000 cycles of heating and cooling.

## Conclusion

Select additives can be added to an electroless copper solution, which decrease the stress of an electroless copper deposit. The reduced stress allows for a blister free copper deposit on smooth, difficult to metallize substrates such as PI. These additives showed no adverse effects on the interconnect reliability of the resulting copper deposit when exposed to thermal stress as evaluated by solder shock and IST. **PCB**

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See Beyond


# Enabling Smart Wearable Technology: Flexible, Stretchable Interconnect

**by Joan K. Vrtis, Ph.D.**
MULTEK TECHNOLOGIES

**Abstract**

Breakthroughs in wearable electronics are driving exciting, innovative applications in the health, wellness, safety and entertainment markets. But as the user experience matures, product design is driven as much by fashion and style as it is by form, fit, and function. The human-centric element has created a paradigm for the printed circuit, interconnect designers and fabricators. No longer is the printed circuit a mechanically static, controlled-environment technology. Now it must survive continuous dynamic stresses brought on by flexing, bending, twisting, stretching and dropping in an uncontrolled use environment. This article highlights the current and forward-looking interconnect technologies enabling the stream of amazing new smart wearable electronic devices connecting the user to their personalized experience.

**Background**

Wearable technology is not new. Anyone who experienced the 1970s remembers the Mood Ring, designed with a thermotropic liquid crystal material inside or surrounding the stone of the ring that changed color as the wearer's body temperature changed. The colors inferred the various moods of the user: blue for calm, violet for happy, black for tense, and so on. The wearer had visual feedback with which they could choose to alter his mood.

The advent of the Internet and the World Wide Web began to revolutionize culture and commerce, initially through instant communication such as electronic mail, instant messaging, voice over Internet Protocol (VoIP), social networking and online shopping. By the late 1990s, physical objects (things) were embedded with electronics, such as software and sensors, and connected to the Internet and thus the Internet of Things (IoT) was born.

According to Gartner Inc., by the year 2020, there will be approximately 26 billion devices on the Internet of Things[1]. In 2014, the Pew

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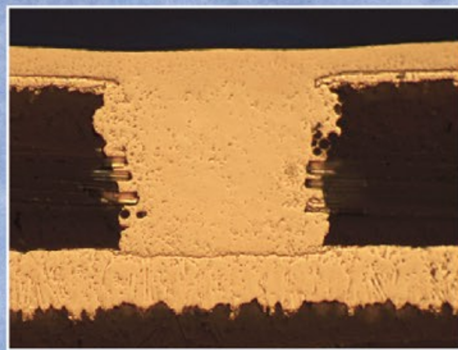

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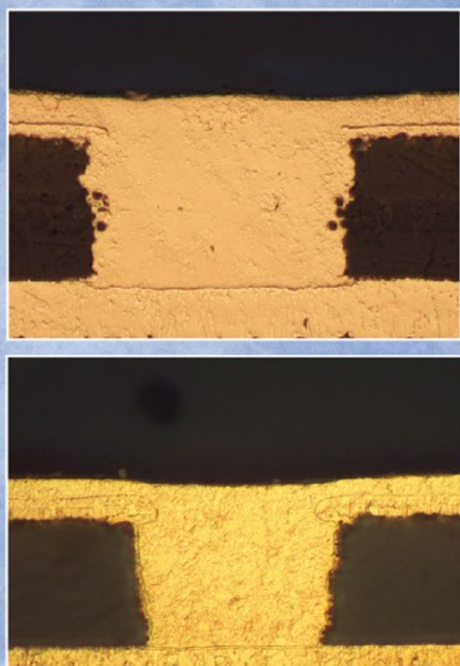

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Research Center Internet Project canvassed technology experts and Internet users about the evolution of embedded devices and the Internet/Cloud of Things by 2025. Eighty-three percent of the respondents agreed that Internet of Things will have widespread and beneficial effects on the everyday lives of the public by 2025[2].

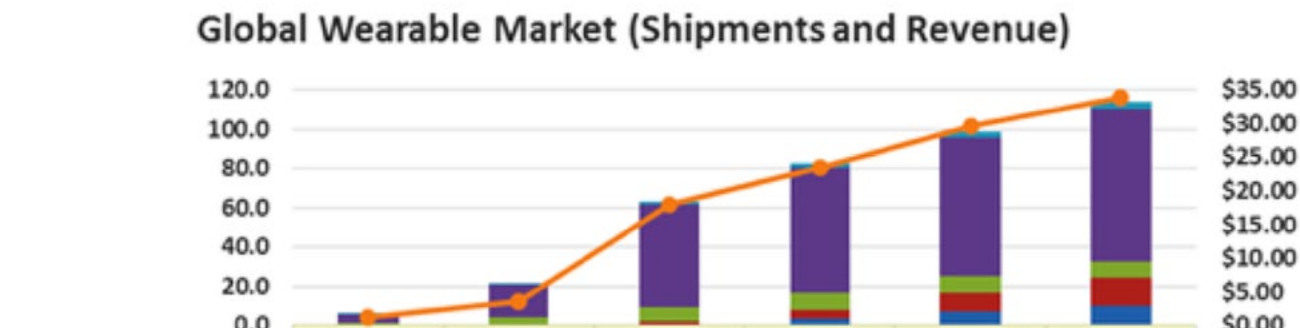
According to the *Global Wearable Technology Market Research Report 2018,* "The global wearable technology market stood at USD 750.0 million in 2012 and is expected to reach USD 5.8 billion in 2018, at a CAGR of 40.8% from 2012–2018. North America is expected to maintain its lead position at 43% of the global wearable technology revenue share in 2018 followed by Europe"[3]. And from the *Wearable Electronics and Technology Market by Applications,* "The overall wearable electronics and technology market is estimated to grow $11.61 billion by the end of 2020 at a compound annual growth rate (CAGR) of 24.56%, from 2014 to 2020"[4]. Based on current market analysis and technology spends, wearable technology is anchored in the future of the IoT.

With the evolution of the IoT, advancements in personal computing technologies have driven printed circuit and printed electronics technology enhancements, power management improvements, wireless module development and overall miniaturization, creating mobile communication devices that fit in the palm of one's hand. The smart phone has enabled personalization of information, social connections and entertainment.

Today, wearable technology has enabled smart, connected devices for personal health and wellness, enhancement of one's safety and the ability to form an individualized entertainment experience. This personal ecosystem is often hubbed by one's smart phone, with information stored on the Cloud and conveniently shared with social networks. The Internet of Things is morphing into the age of the "Intelligence of Things™." As more and more wearable electronics connect to the Internet and provide electronic feedback to support our health, wellness, safety and entertainment decisions, this phenomenon is driving the next age—one of smart, connected living. Figure 1 highlights the estimated shipments and revenue by wearable technology application.

### Advancements in Interconnect Design and Materials

Over the past few decades, the computer industry sifted into various subcategories—PCs,




| | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 |
|---|---|---|---|---|---|---|
| Other | 0.3 | 0.5 | 1.7 | 2.4 | 2.9 | 3.8 |
| Wristwear | 4.5 | 16.5 | 52.5 | 64.3 | 71.0 | 77.8 |
| Modular | 1.4 | 4.1 | 6.7 | 8.2 | 8.3 | 8.0 |
| Eyewear | 0.0 | 0.0 | 1.6 | 4.5 | 9.9 | 14.7 |
| Clothes | 0.0 | 0.0 | 0.6 | 3.6 | 6.8 | 9.6 |
| Total Revenue ($B) | $1.20 | $3.60 | $17.90 | $23.50 | $29.70 | $33.80 |

Figure 1: The global wearable market[5].

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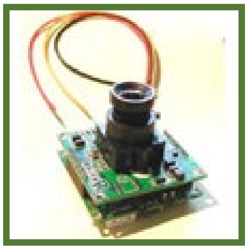

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laptops, tablets, etc. So, too, are wearable electronics becoming categorized, not so much by function as by proximity to the user. Wearable electronics are designed into many forms for body adaptation such as a wristband, apparel, footwear, jewelry, patches, earwear and eyewear. The proximity of the wearable electronic to the user is often categorized into three areas reflecting the level of body contact by the product: close to the body; on the body; and in the body. Figure 2 depicts the wearable electronics body contact level and type of product per category.

With any new technology, eventually certain standardizations become clear. The development of technology building blocks has enabled some manufacturers to develop smart component strategy and accelerate their time to market for certain products.

In creating a wearable electronic product, seven technology building blocks are considered: security and computing; sensors and actuators; human machine interface; connectivity; smart software; battery and power; and flexible technologies and miniaturization. Figure 3 depicts the technology building blocks for wearable electronic products.

## Flexible Technologies

Flexible interconnect technologies and component miniaturization are enabling the wearable electronics market. The vast majority of wearable electronic products have printed circuits or printed electronics. There is a distinct difference between these interconnect technologies. The choice of a printed circuit versus a printed electronics technology in a wearable device is driven by form, fit, function and cost. The design and material combinations thereof can thus provide rigid, flexible and/or stretchable electronic solutions.

Rigid PCBs, flexible printed circuits (FPCs), and rigid-flexible circuits (RFPCs) are considered printed circuit technologies. PCB, FPC and RFPC are primarily fabricated using conventional methods of circuit formation of electrical interconnect features by etching copper sheet and lamination with dielectric materials[6]. High-density interconnects (HDI) and every-layer interconnect connection (ELIC) PCBs combined with FPCs form a complex RFPC are more recent technologies that have enabled higher functionality demanded of advanced smart connected wearable devices[7]. Figure 4

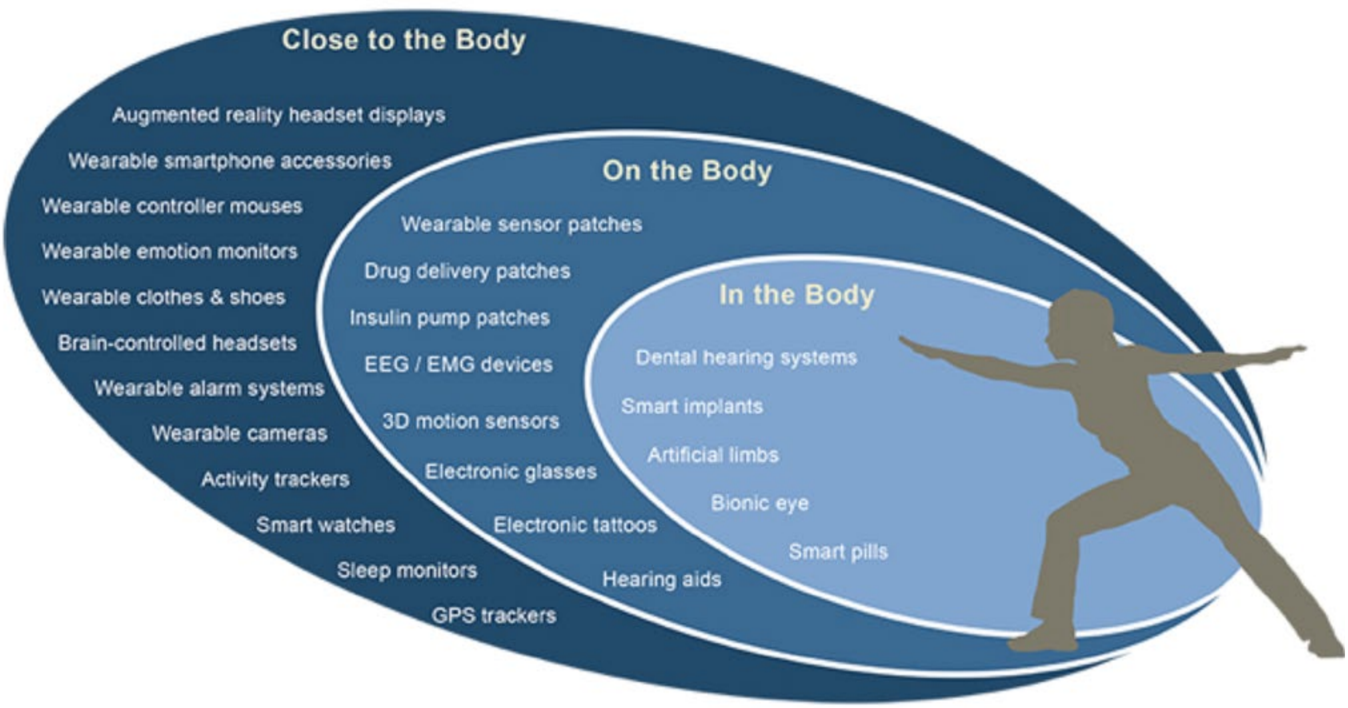


Figure2: Proximity categories of wearable technology. (courtesy of Multek Technologies Ltd.)

represents an RFPC. This figure illustrates a multifunctional rigid board capable of being folded over on itself, reducing the size to a very small stacked package.

Printed electronics utilize printing methods such as screen printing, gravure, and inkjet printing to create interconnects on various substrates. Conductive inks and pastes are used as the electrical circuit material pattern that is deposited onto the substrate. Printed electronics may often be less expensive than printed circuits due to processing and materials although complexity in design and performance drive the costs. Printed ink resistance or frequency characteristics are different from solid copper. In deciding to use printed electronics, the semiconductor component operating voltage and impedance-related (or transconductance) de-


Figure 3: The technology building blocks of wearable electronics. (courtesy of Flextronics Corp.)

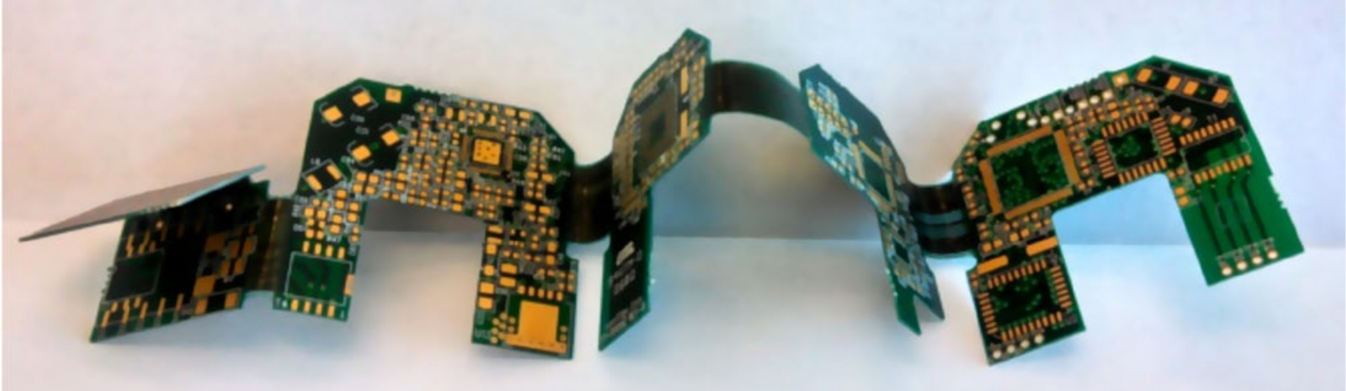

Figure 4: Rigid-flexible printed circuit.

sign requirements must be understood. Also, for any wearable device, the materials' exposure compatibility with the human body surface and fluids must be comprehended, especially for on-the-body and in-the-body applications.

Referring earlier to the proximity categories (Figure 2), the choice of interconnect technology, design and material is defined by these categories. FPCs, RFPCs and printed electronics technologies are often used to take advantage of the flexibility requirements in wearable electronic devices. There are two ways to incorporate these technologies.

1. Flex to fit: The circuit is flexed once only to fit into the assembly.
2. Dynamic flex: This circuit will not only flex to fit into the assembly, but will be dynamic during operation[8].

Multiple applications in each proximity category have high mechanical demands on the interconnects. For example, interconnects in a wristband application must account for constant flexing and twisting during frequent application and removal from the wrist. The electronic patch (electronic tattoo), adhered to the skin, must move with the body, withstand human sweat, moisture and temperature during bathing and daily use. In each example, dynamic stresses are evident.

### Stretchable Electronics

Advances in design and materials allow for stretching of the interconnects to mitigate the higher stresses and strains experienced by the circuit in certain wearable devices. In FPCs and RFPCs, higher ductility copper and optimizing the elongation of the dielectrics often addresses the interconnect reliability required. There are more harsh dynamic stress and strain conditions observed in a hinge area of smart eyewear, movement of smart apparel, or in soles of smart shoes. In these cases, the FPC and RFPC can be designed to stretch. The design employs meandering sections to allow a stretching and twisting movement. Figure 5 depicts a meandering design as one of many interconnect design options. The current challenge of designing a meandering structure is the limitation of commercial PCB/FPC design layout software to provide ease of use meandering solutions. The majority of the stretchable interconnect design software is proprietary and specific to a small application range.

In printed electronics, several advances in pastes, inks and substrates are supporting the advancements in stretchable solutions. Polyesters and polyimides are common substrates for printed electronics.

Elastomeric substrates such as polyurethane and polydimethylsiloxanes are providing stretchable options. Silver inks form the majority of the conductive circuits in printed electronics applied to stretchable substrates. The advanced nanoparticle technology of these inks supports a degree of movement of the interconnect. Figure 6 illustrates silver printed ink patterned on an elastomeric substrate.

Stretchable electronics may combine traditional printed circuits and printed electronics. For example, multiple PCBs can be connected

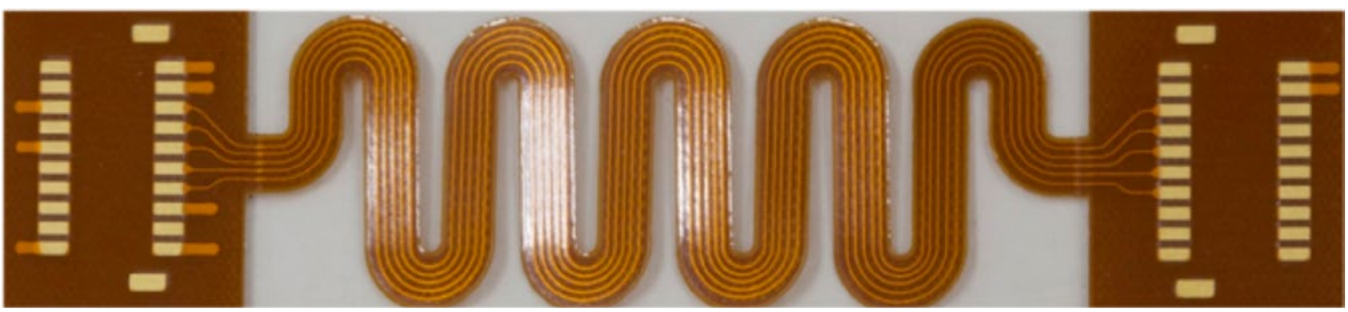

Figure 5: Flexible printed circuit designed with meander for stretch and twist. (courtesy Multek Interconnect Technology Center)

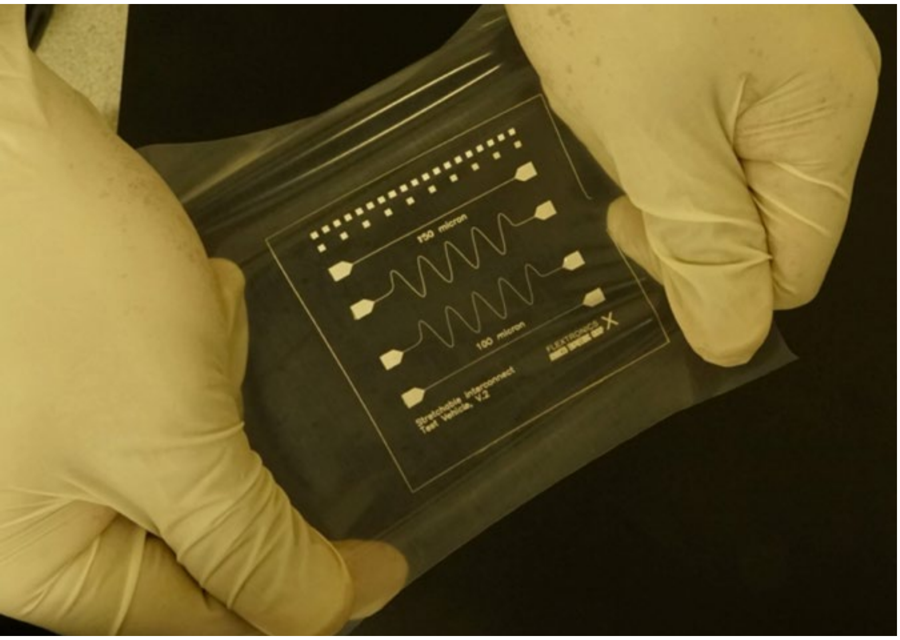


Figure 6: Example of a stretchable printed electronic circuit, with Ag printed ink patterned on elastomeric substrate. (courtesy of Flextronics Advanced Engineering Group)

in a matrix with stretchable copper conductors similar to Figure 5 where the PCBs act as functional islands where the surface mount components are adhered and then the entire PCB island matrix is encapsulated with a protective elastomeric material. This design affords the entire system to be stretchable. The final wearable device may be used for close-to-body or on-the-body applications.

As explained by Wagner and Bauer[9], design configurations for stretchable circuits includes waves, meanders, conductive particles embedded in an elastomeric matrices, meshes and other. The design challenges include protecting the stretchable circuit from exceeding its elongation to break. The solution is to design the wearable device as a stretchable system.

## Summary

As breakthroughs continue in wearable technology, any one of these interconnect technologies could leapfrog past the others in terms of usability and applicability. Printed circuits and printed electronics have advanced wearable technology market. These interconnect technologies have enabled the growth of stretchable electronics solutions. The future of flexible and stretchable circuit technologies will require advancement in materials, standardized commercial design software and equipment for advanced assembly and a broad systems understanding by the product designers to account for continuous dynamic stresses and strains brought on by flexing, bending, twisting, stretching and dropping in an uncontrolled use environment. **PCB**

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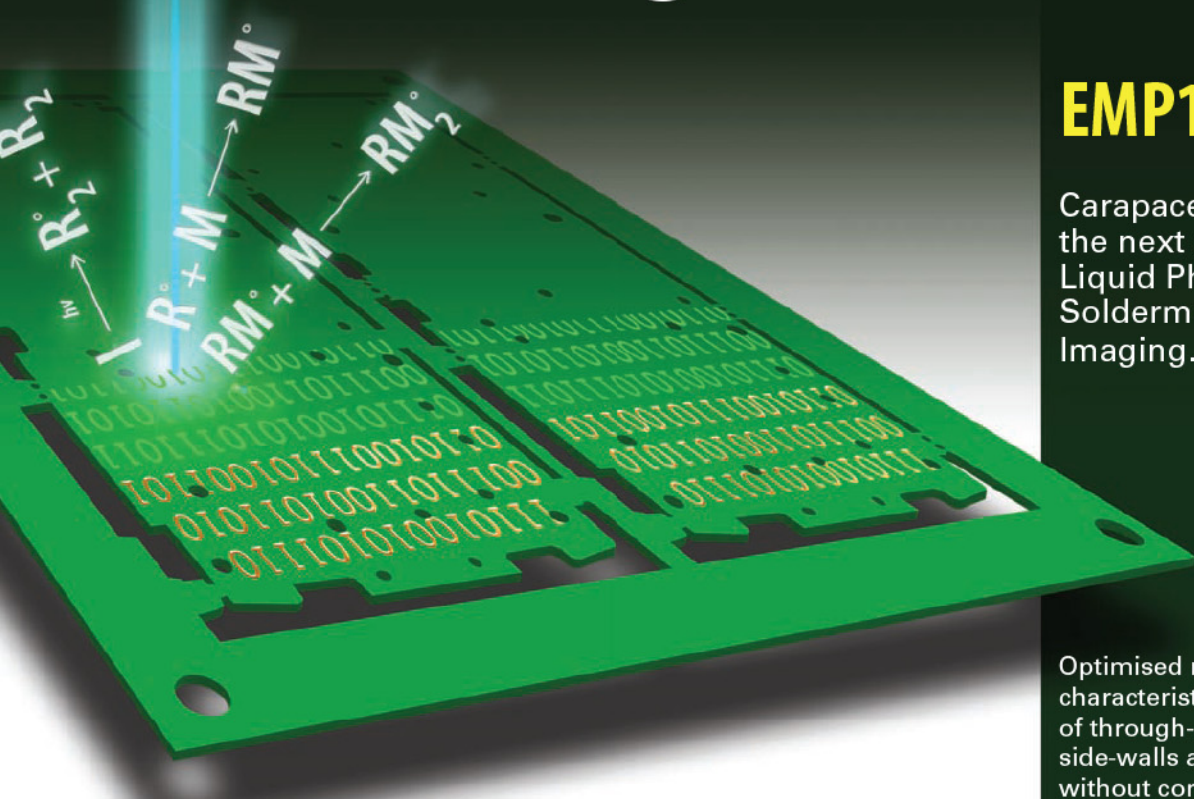

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# Flexible and Stretchable Circuit Technologies for Space Applications

**by Maarten Cauwe, Frederick Bossuyt, Johan De Baets, and Jan Vanfleteren**
LABORATORY FOR ADVANCED RESEARCH IN MICRO-ELECTRONICS (IMEC) GHENT UNIVERSITY, BELGIUM

**Abstract**

Flexible and stretchable circuit technologies offer reduced volume and weight, increased electrical performance, larger design freedom and improved interconnect reliability. All of these advantages are appealing for space applications. In this paper, two example technologies, the ultra-thin chip package (UTCP) and stretchable moulded interconnect (SMI), are described. The UTCP technology results in a 60 µm thick chip package, including the embedding of a 20 µm thick chip, laser or protolithic via definition to the chip contacts and application of fan-out metallization. Imec's stretchable interconnect technology is inspired by conventional rigid and flexible printed circuit board (PCB) technology. Stretchable interconnects are realized by copper meanders supported by a flexible material (e.g., polyimide). Elastic materials, predominantly silicone rubbers, are used to embed the conductors and the components, thus serving as circuit carrier. The possible advantages of these technologies with respect to space applications are discussed.

**1. Introduction**

The driving application for flexible and stretchable circuit technologies is consumer electronics, especially handheld and mobile devices, which benefit the most from the reduction in form factor, the increased functional density and enlarged user comfort that is made possible with these technologies. Reduced volume and weight, increased electrical performance, larger design freedom and improved interconnect reliability are benefits that are also appealing for space applications.

Traditionally, electronics and sensor circuits are fabricated on flat rigid substrates, like FR-4 PCBs. In this conventional technology, pack-

aged integrated circuits (ICs) and passive components are assembled onto the rigid PCB by soldering. For many applications, especially for mobile, portable, wearable and implantable electronics, the circuit should preferably be seamlessly integrated into the object that is used for transportation, is carried along, or worn on or inside the body. The electronics should be comfortable and unnoticeable to the user. In general, standard circuits do not fulfil these requirements. The user comfort can be increased in two ways. Extreme miniaturisation of the circuit reduces the presence of the system. A second approach is to transform the flat rigid circuit into a three-dimensional, conformable variant, following the random shape of the object or body part onto which it is integrated.

In this contribution, two original technologies developed at imec-CMST are presented. The ultra-thin chip package (UTCP) technology embeds 20–30 µm thick chips in a stack of spin-on polyimide (PI) layers. Adding thin-film, fan-out metallization results in an extremely miniaturized, lightweight and flexible chip package with a total thickness below 100 µm. Next to flexible electronics, a number of technologies for dynamically or one-time deformable stretchable circuits are under development. The stretchable concept is based on the interconnection of individual components or component islands with meander shaped metal wirings and embedding in elastic polymers like silicone rubbers (PDMS), polyurethanes (PU) or other plastics.

Although these technologies were not explicitly developed for space applications, their unique features create the potential for use in this new application domain. Miniaturization through UTCP use and 3D integration through circuit random deformability significantly reduces system size and weight, which is an important advantage for space applications. An interesting point of view, further discussed in this paper, is the possible improvement in interconnect reliability that these new technologies offer. Thanks to the embedding in elastic materials, stretchable circuits could show a decreased sensitivity to vibration. UTCPs can be embedded in flexible or rigid PCBs using lamination, through-hole drilling, and via metallization. UTCP production and PCB embedding is completely solderless, thus avoiding associated reliability problems, usually encountered in harsh environments.

The following two sections describe the process flow and application examples for flexible chip packaging and stretchable electronics. Section 4 discusses the advantages these technologies can offer for space applications.

## 2. Flexible Chip Packaging

One of the main drivers in packaging research is to integrate as much functionality into a single package as possible, without increasing the overall size of that package. The ultimate goal is a system-in-package (SiP), where both active and passive components are integrated, realizing a standalone (sub)system with a given functionality. One of the current challenges is to match this increase in functional density with improved flexibility and reduced overall thickness. A key aspect herein is the use of thinned bare-die Si chips to minimize the package form factor.

Looking purely at the functional density, several SiP approaches can be applied to realize the high-density modules. Fan-out wafer-level packaging (FOWLP), where the package is reduced to its absolute minimum, and direct chip embedding are two examples of technologies that offer increased functionality in a reduced form factor. A European representative of the latter technology is described in the next section.

The overall thickness of these packages, however, remains in the order of hundreds of

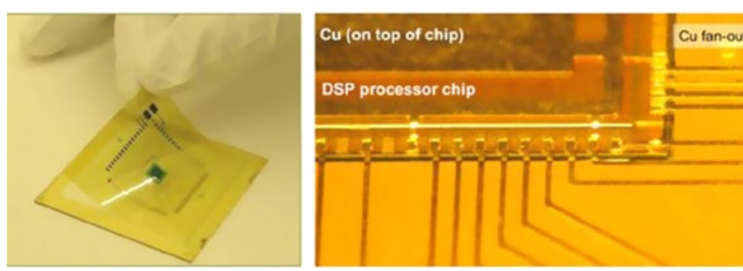


Figure 1: Overall view of the ultra-thin chip package (left) and close-up of the fan-out circuitry (right).

micrometres, strongly limiting the flexibility of the substrate onto which they are placed. The ultra-thin chip packaging technology described later combines a high degree of miniaturization with an inherently flexible chip package. The use of thin-film processing makes it possible to integrate chips with the highest complexity and a fine contact pad pitch.

### Chip Embedding

The Embedded Component Packaging technology from AT&S directly integrates the components in the core layers of the PCB[1]. The technology can be used for the embedding of both active and passive components. The main characteristics of the technology are the use of openings in the prepreg layers matching the location of the components and the microvia interconnections to the contact pads of the embedded component. The plated Cu microvia interconnection eliminates the need for solder or conductive adhesives, thus avoiding the associated failure modes. The thickness of the components (100–150 µm for chips, 150–300 µm for passive components) and their pad metallization (copper) need to be compatible with the lamination and metallization process steps, respectively. A broad range of embeddable passive components are currently available and manufacturers are continuously improving their product range with respect to available values, tolerances, and temperature and power ratings. Bare-die chips are more difficult to procure, especially for lower volumes, but are becoming more and more common.

A standard PCB process flow starts with a double-sided core, which is structured in the subsequent process steps and built up to a multilayer construction. In the case of embedding components, a so-called "embedded core" is produced in the first phase of the process flow. The main process steps for embedding of components are printing of adhesive, assembly of components, lamination and drilling of vias and plated through holes. The suitability of embedding passive components for space applications is currently being investigated in the PCESA project (ESA/TRP) by imec, AT&S and QinetiQ Space.

### Ultra-thin Chip Package

To achieve the requirements of form factor and flexibility, the total thickness of the chip package needs to be reduced by an order of magnitude (i.e., less than 100 µm). A suitable candidate is the ultra-thin chip package (UTCP) technology, developed and patented by imec-CMST[2, 3]. This technology consists of an ultra-thin chip, embedded in polyimide layers and contacted using microvias and a fan-out interconnection scheme (Figure 1).

Figure 2 shows the process flow for realizing the UTCP. The process starts from a glass carrier substrate with a suitable release layer, onto which a polyimide layer is spun. The ultra-thin chip, with a thickness down to 20 µm, is subsequently placed in the desired location. A second photosensitive polyimide layer is spun on top of the chip and consequently patterned to remove the polyimide in the area above the chip. The second polyimide layer thus acts as a planarization layer for the third polyimide layer that carries the interconnection circuitry. This metal layer is realized by vacuum depositing a copper seed layer which is electroplated to the desired thickness. As a final step, the metallization layer is patterned, resulting in a flexible interposer

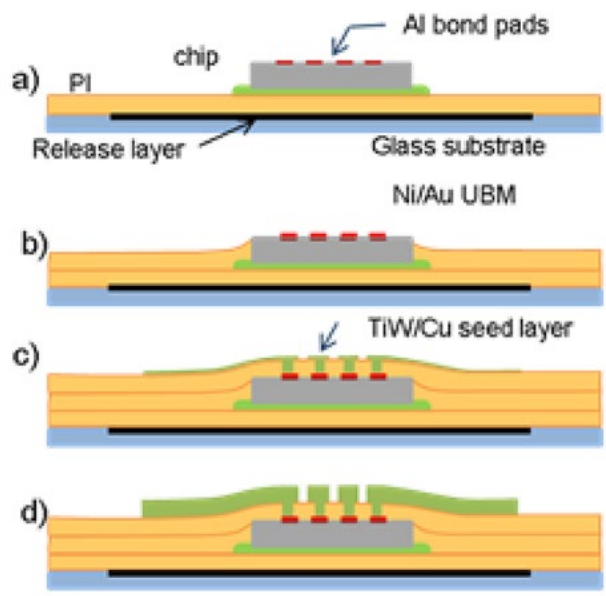


Figure 2: Process flow for realizing the ultra-thin chip package.

with a thickness of about 70 µm, mounted on a glass carrier. The design of the metal fan-out allows converting the fine pitch (currently down to 65 µm) of the IC to a larger pitch compatible with the intended application, such as embedding or stacking. Furthermore, it is possible to create interconnections between several contact pads of the IC, reducing the required number of connections to the external substrate.

The embedded die can be used as a package (e.g., solder balls can be placed on the contacts and the package can be solder assembled on interconnection substrates). Alternatively the ultra-thin package can be embedded in a stack of rigid or flexible PCB layers. The UTCP can be tested before embedding, presenting a clear advantage compared to the direct embedding of bare dies.

Figure 3 shows a schematic process flow for UTCP embedding, in this case between two polyimide copper-clad laminates. The UTCP is aligned to the copper pattern on one of the inner layers and encapsulated by the acrylic adhesive that is generally used for building multilayer flexible printed circuit boards. After lamination, holes are drilled though the stack and consequently metallized, realizing the interconnection between the UTCP and the board without needing microvia interconnection schemes. The embedding of UTCPs has been demonstrated for a number of flexible and rigid materials, which need to offer good adhesion to the polyimide-based UTCP and be compatible with the through-hole metallization process.

A cross-section of the resulting board with embedded UTCP is shown in Figure 4a. A UTCP of a RF transceiver (ZL70102 from Microsemi) is embedded in a three-layer flexible printed circuit board (FCB). The plated through-hole interconnecting layer 1 and 3 of the FCB to the UTCP can be seen on the right-hand side. The total thickness of the FCB averages around 250 µm.

Embedding the UTCP package inside the board not only avoids the use of bulky surface-mount packages, but also frees up board space for mounting active or passive component. This three-dimensional packaging approach allows for a significant reduction in board size and thickness. As an example, Figure 4b shows a comparison between an embedded UTCP radio module and the original module based on a chip-scale package (CSP). The total volume of the module is reduced to less than 60% of the original.

Further miniaturization can be realized by integrating multiple ICs in a single package. This can be done by stacking multiple UTCP-packaged dies on top of each other using lamination

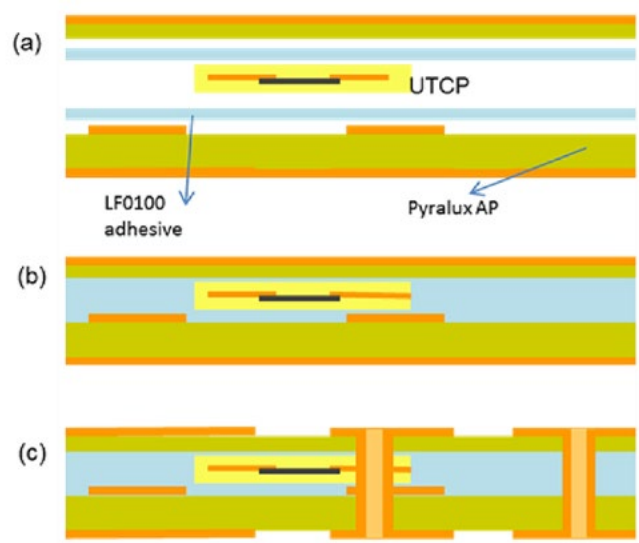


Figure 3: Schematic process flow for UTCP embedding.

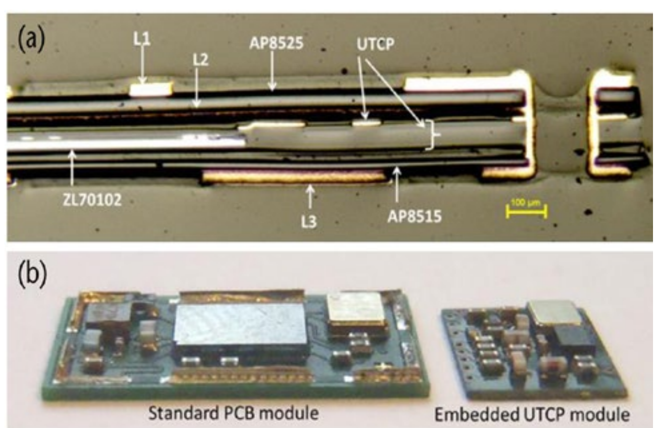


Figure 4: A cross-section of a board with embedded UTCP of a RF transceiver (ZL70102 from Microsemi, top) and the comparison between the embedded UTCP radio module and the original module (bottom).


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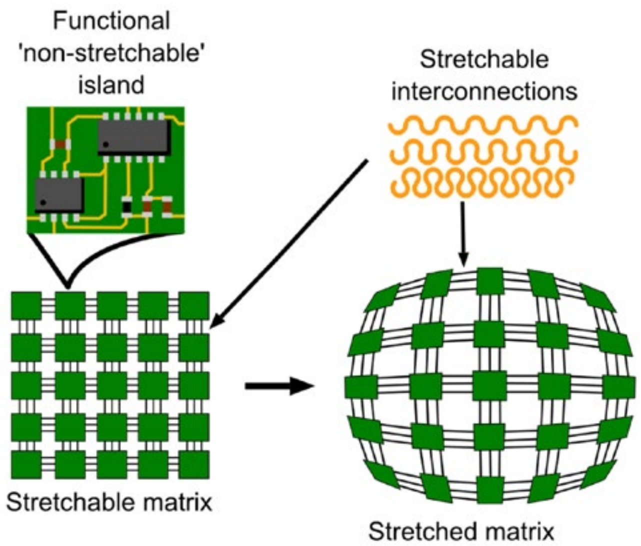


Figure 5: Overall concept of a stretchable circuit.

technology, combined with the fabrication of the interconnections between the layers using via drilling and metallization by electroplating. Such a stacked UTCP is not flexible anymore, but an extreme degree of miniaturization is realized: in a package of about 300 µm thick, four dies can be embedded and interconnected[4].

### 3. Stretchable Electronics

The overall concept of a stretchable circuit is illustrated in Figure 5. The circuit is comprised of a number of rigid (or moderately flexible in some cases) component islands, where each island holds a single component or a limited number of components. The individual rigid components or component islands are interconnected, not by straight Cu lines, as in conventionally designed PCBs, but by means of meander shaped Cu conductors instead. Once the meanders have been embedded in a mechanically elastic circuit carrier, they can dynamically elongate (stretch) under mechanical forces and come back to their original state, without losing their electrical interconnection function during this stretching. The meander shape in combination with the elastic carrier makes the conductor function as a two-dimensional spring. Realizing the planar meanders using the stretchable moulded interconnect (SMI) technology developed by imec and Ghent University, requires only a minimal deviation from conventional PCB processing.

The first steps in the SMI process flow are shown in Figure 6. A rigid carrier substrate is covered with a temporary adhesive, onto which a copper foil or polyimide-copper flexible laminate is mounted by lamination. The optional polyimide layer serves as support material for the copper meanders and for the component islands. Supporting the meanders with a PI carrier has proven to greatly improve the mechanical reliability and operational lifetime of the copper meander circuits.

Next, the samples go through a number of standard PCB manufacturing and assembly steps. Copper meanders, along with the standard design interconnections on the component islands, are patterned by photolithography and wet etching. The polyimide support layer is structured by laser cutting. If necessary, solder mask is locally applied by screen printing,

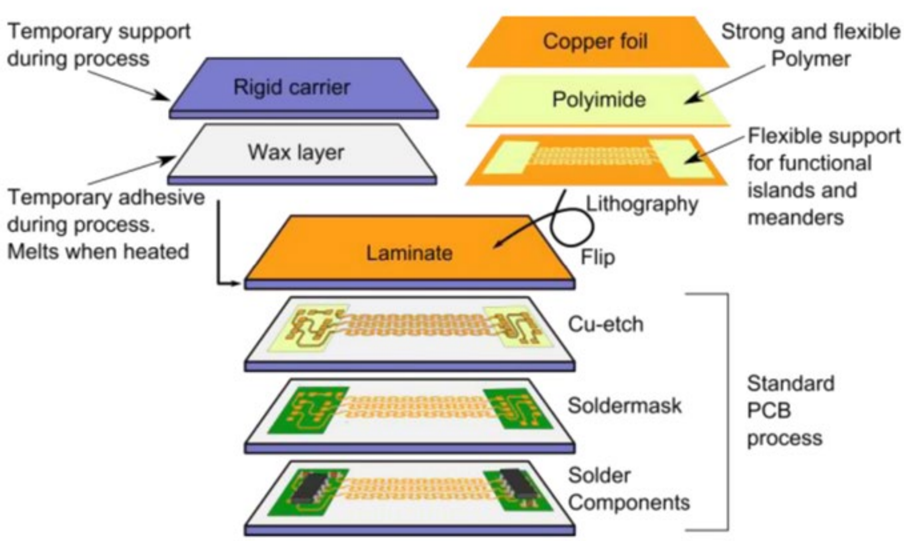


Figure 6: First part of the SMI process flow.

contact pad finish is applied and components are mounted using a conventional reflow solder process. At this point, the circuit can be tested and repaired, if required. Figure 7 shows an SMI substrate after component assembly.

The second part of the SMI process flow involves the application of the stretchable carrier material, giving the circuit its resilience (Figure 8). In the first step, the top of the circuit is covered by a layer of stretchable material by liquid injection moulding (LIM) of a two-component polydimethylsiloxane (PDMS) mixture. Alternatives for the application of the stretchable carrier material by LIM include cover lamination and spray coating. Besides PDMS, also polyurethane (PU) or any polymer for which a liquid precursor or a thermoplastic variant is available can be applied. In a second step, the assembly is removed from the temporary carrier. After cleaning, the circuit is completely embedded by

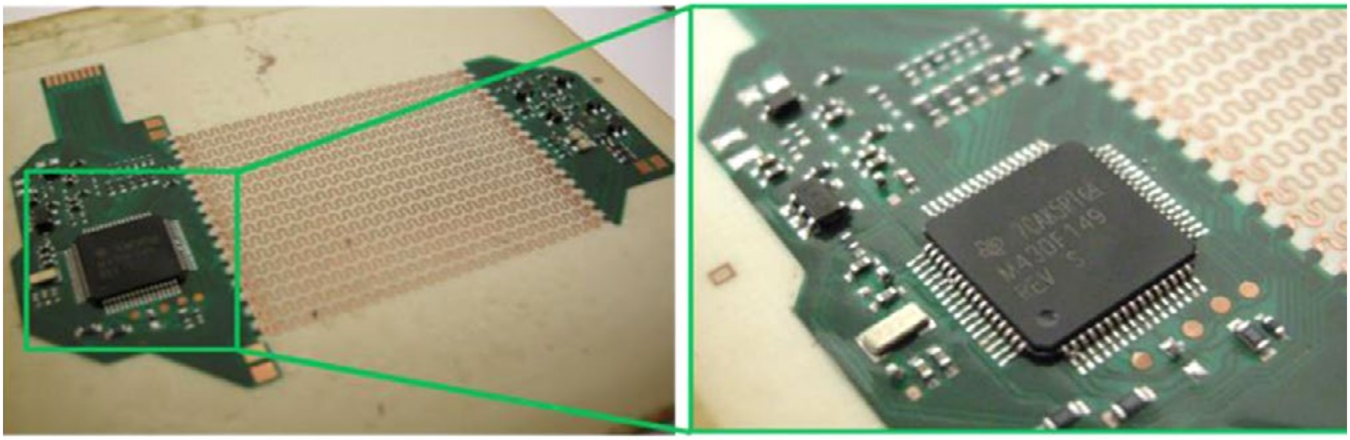

Figure 7: Example of a stretchable system for respiratory monitoring before encapsulation.

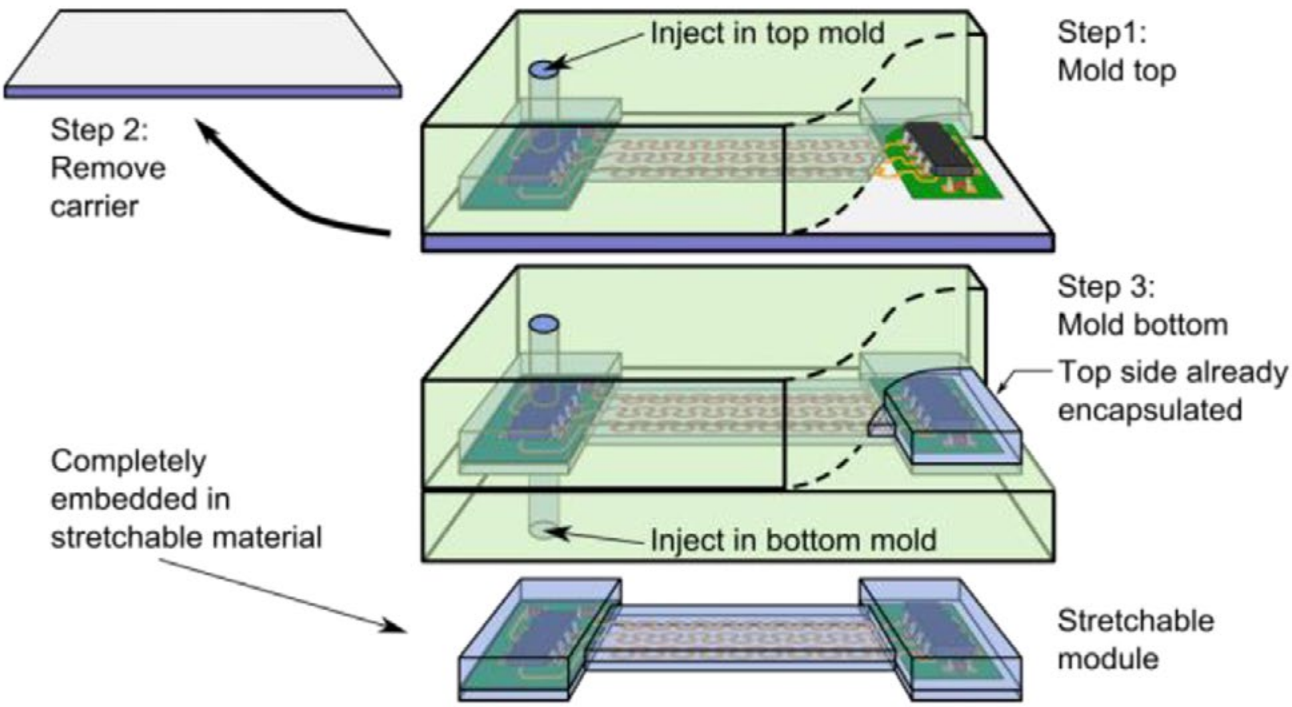


Figure 8: Second part of the SMI process flow.

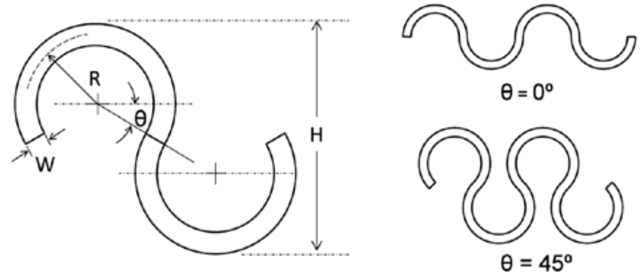


Figure 9: Horseshoe shaped meander with relevant design parameters.

applying a second layer of stretchable material at the bottom (i.e., by a second LIM step).

A critical factor in the use of stretchable interconnections is the design of copper meanders. Extensive modelling was performed to minimize stress and strain concentrations in the meander under deformation. The current meander shape of choice is the horseshoe shape, as shown in Figure 9. A horseshoe-shaped meander is a connection of circular segments, offering a good compromise between sufficient stress distribution along the meander on one hand, and ease of design and circuit layout on the other. For minimal stress the width (W) of the track should be as small as possible. The minimum width is determined mainly by technological constraints. During the cycling elongation of the stretchable circuit, a permanent deformation or plastic strain is induced in the metal causing a fatigue failure. Therefore, in order to improve the fatigue reliability of the stretchable interconnect; the plastic strain has to be minimized.

The ratio R/W determines the maximum plastic strain in the meander for a given deformation. In general for deformations of 20% and less, the maximum plastic strain decreases with increasing R/W. High R/W ratios, however, also mean meanders with high overall width, and thus a low density of parallel running meanders. A ratio of R/W = 10 normally offers a good compromise between low maximum plastic strain in the meander and high number of parallel running meanders per unit width of the stretchable interconnect area.

A further improvement of the mechanical reliability of the meanders is achieved by supplying the meanders with a flexible support, i.e., a PI film. Numerical modelling showed that the PI width is the main parameter, reducing the maximum plastic strain in the Cu meander[5].

Focus of the reliability investigation for stretchable interconnections has been on the optimization of the performance under mechanical stress like (e.g., periodic or random deformation of the circuit). No standard tests for stretchable circuits exist today. In order to quantify and assess the mechanical reliability of stretchable circuits uniaxial stretching tests are executed on samples that contain a number of parallel running meanders. The main test is cyclic stretching at moderate maximum elongation until conductor rupture.

Results of these cyclic stretching tests have been described extensively elsewhere[6]. The main conclusions are that supporting the Cu meanders with a flexible material like polyimide drastically improves the lifetime of the interconnection. As an example, a double sided PI-enhanced stretchable interconnect withstands more than 90,000 stretching cycles at 5% elongation, and even for elongations up to 20%, the PI-enhanced stretchable interconnect can survive more than 400 cycles.

Proper design and fabrication of the transitions between component islands and the stretchable interconnects is at least as important as the stretchable interconnects themselves. There is no quantitative structural design rule or optimized design available for solving this reliability issue. A qualitative rule is that the transition from rigid over flexible to stretchable circuit parts should be as smooth as possible.

Optical microscopy was used to analyse both types of samples after the endurance test. The copper interconnects break at the top of the meanders, which is the place where the highest accumulated plastic strain is present[7]. The start of the micro crack as seen in Figure 10 is not detected by the resistivity measurements due to the very low increase of resistivity. On non-supported copper tracks, the crack propagates during one or just a few cycles leading to the sudden breakdown. Delayed crack propagation is observed for the meanders with PI support, which translates in a slowly increasing track resistance.

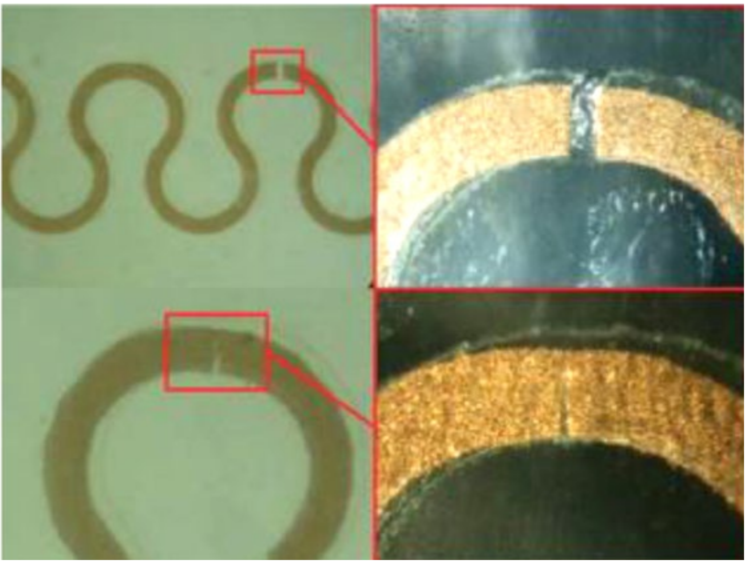

Figure 10: Failures at the top of meanders with polyimide support. Upper picture shows complete fracture of the copper trace, while the bottom picture shows an initiated microcrack.

## 4. Relevance to Space Applications

The need for thin, flexible packaging and stretchable interconnection is driven by the desire for increased functional density in a reduced or application-specific form factor. Reliability requirements for the typical use environments are not of the highest concern during the technology development phase. The improvements offered by these new technologies, such as increased functional density, form factor reduction and the possibility to adapt to any shape, are also interesting for space applications. In this application field, however, excellent reliability is an absolute priority.

From this point of view, it is interesting to evaluate what reliability improvements these new technologies could bring. Failure mechanisms for solder interconnections are well-documented[8, 9]. Although no legislative obligation is in place, lead-free solder issues become more and more relevant for space as well[10, 11]. Based on the Pb-free experience in consumer applications, failures related to the use of solder will only increase with this transition. Embedding of components in general, and of UTCPs in particular, offer a promising alternative by using plated interconnections in the form of copper microvias or plated though-holes. Both from a dimensional as from a material point of view, these interconnections have a thermo-mechanical advantage over bulky and brittle solder joints. Embedding the components inside the board also offers increased mechanical protection with respect to bending or shock.

By its very nature, stretchable interconnections offer an even larger potential for mechanical robustness. By dividing the large system into smaller sub modules that are interconnected by elastic interconnections which can absorb the mechanical stress from vibrations or shock, sensitive components can be protected without the need for bulky anti-vibration frames.

The authors are well aware of the fact that these statements are oversimplified and that the proposed technologies will suffer from or even introduce new failure modes. Then again, it is thinking outside of the box that put a man on the moon.

## 5. Conclusion

Two emerging technologies for flexible packaging and stretchable interconnections were discussed in this paper. The UTCP technology makes it possible to realize chip packages with a total thickness of less than 100 µm. Embedding these packages to exploit the third dimension results in a volume reduction of more than 60%.

Stretchable interconnections in the form of encapsulated meanders can survive tens of thousands of stretching cycles of up to 5% elongation. It has been illustrated that mechanical reliability is strongly enhanced by introducing a flexible support material for the meanders and by providing smooth mechanical transitions between the rigid solder assembled standard components and the soft and conformable stretchable interconnects.

Compared to common assembly and interconnection technologies for space applications, the proposed technologies are still in their infancy. The possibilities for new form factors with increased functional density are obvious, but also a potentially improved reliability in harsh environments merits further investigation into applying these technologies to space applications. **PCB**

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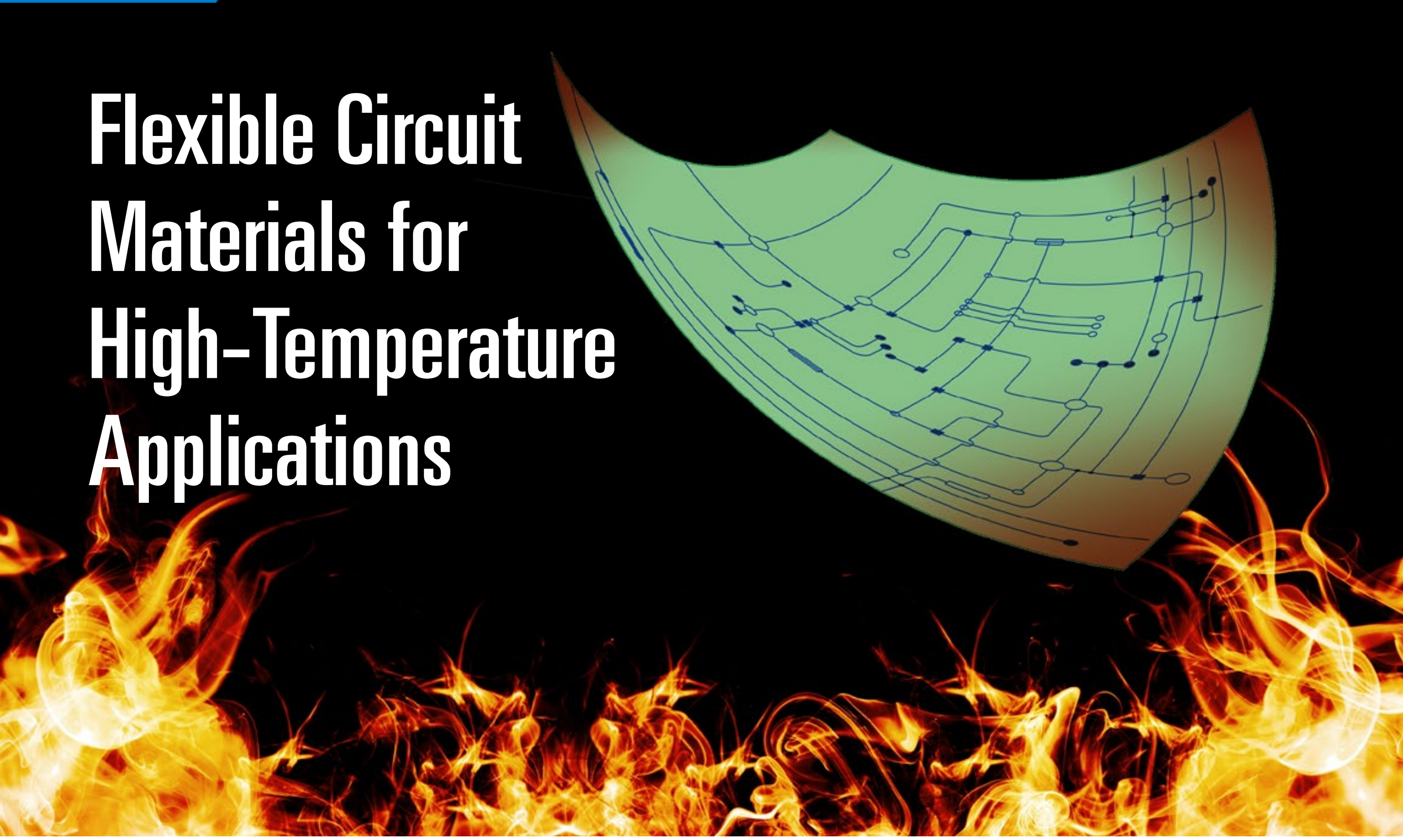
# Flexible Circuit Materials for High-Temperature Applications



**by Sidney Cox**
DUPONT CIRCUIT AND PACKAGING MATERIALS

**Abstract**

Many opportunities exist for flexible circuits in high-temperature applications (automotive, military, aerospace, oil and gas). Flex circuits in these applications have been hindered by a lack of materials that can survive higher temperatures. Some materials, especially some thermoset adhesives, break down over time at higher temperature, becoming brittle or losing adhesion to copper. Polyimides tend to perform much better under high temperature.

The other issue is the lack of good test methods to verify that flex materials can survive higher temperatures. Several methods for testing copper clad laminates exist, but there are very few for coverlays and bondplies. We will discuss different test methods for measuring high-temperature capability including the new IPC service temperature test. We will also report on test results for various flexible materials and our recommendations for the best flexible materials for high temperature applications. This will include development work on new flex materials for high-temperature applications.

**Introduction**

More applications require flexible circuits that must survive high-temperature environments. These include automotive applications near the engine, oil and gas down-hole pumps, and aerospace applications near jet engines. There have been limited test methods to determine what temperatures flexible materials can survive.

The damage caused by high-temperature environments will mainly fall in three categories: loss of adhesion between copper and dielectric, loss of adhesion between dielectric layers, and embrittlement of the dielectric layers. At the highest temperatures the copper would also become brittle, but in most cases the flexible circuit dielectrics fail first. Thermoset adhesives seem to be most sensitive to embrittlement especially compared to polyimide films which are much more resistant to high temperatures.

UL has two different temperature ratings. The RTI (relative thermal index) is based on the temperature aging of base dielectrics. For flex

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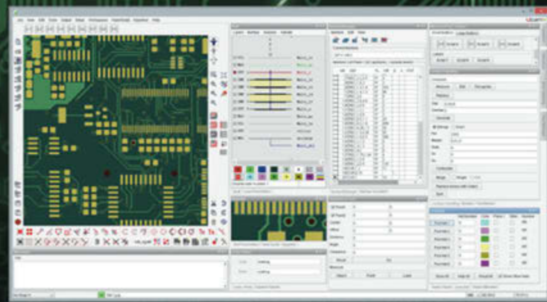

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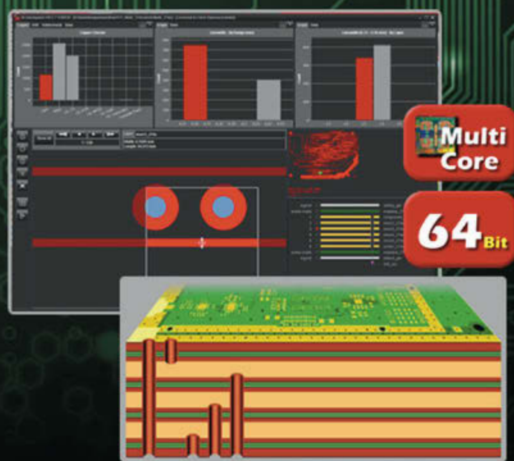


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materials this is mainly polyimide films. The RTI is determined by loss of tensile strength (mechanical property) and dielectric strength (electrical property) with long-term thermal aging. The RTI tests only measure the degradation of the base film properties. The samples are tested declad (without copper) so it does not capture copper adhesion loss aspects of thermal aging. So RTI by itself is not a good measure of the capability of a copper clad laminate.

The UL MOT ratings are assigned for copper clad laminates and primarily measure the loss of copper adhesion to the adhesive layer. The MOT uses accelerated heat aging. MOT is mainly used for rating copper clad laminates. The UL MOT cannot be higher than the lowest of the mechanical or electrical RTI.

A new IPC test method has been developed to measure service temperature (IPC-TM-650 2.6.21B) and was originally created specifically for flexible copper clad laminates. It was later revised to allow measurement of service temperature of bondplies and coverlays. The test measures loss of copper adhesion and dielectric strength with high-temperature aging, but does not use accelerated aging; it measures property loss after 1000 hours of aging at the target temperature. The test method is still new and not much data has been reported from this test until now.

### Flexible Clad Testing Results

We have completed testing of flexible copper clad laminates with the IPC service temperature test, and after testing at multiple temperatures, we determined a tentative service temperature rating for most of our clads. The test measures peel strength after 1000 hours of aging. If the final peels are more than 50% of the starting peels then the material achieved a rating at that temperature. Table 1 shows the percent drop in peel strength after 1000 hours for multiple clads and aging temperatures. A, L, T and F are all commercial products. X and D are experimental polyimide films that were laminated to form copper clad laminates.

The three all-polyimide films all show very high service temperature (A, X and D). For all three films, copper foil was laminated directly to the polyimide, so no thermoset adhesive is present in these constructions. The samples that used adhesives to bond the copper foil to the polyimide core all had lower performance (L, F and T). Based on all the testing done so far,

| Flex Clad Type | 105 C | 125 C | 150 C | 180 C | 225 C |
|---|---|---|---|---|---|
| A | N/A | N/A | 100% | 98% | 93% |
| X | N/A | N/A | N/A | 109% | 92% |
| D | N/A | N/A | 95% | 92% | 88% |
| L | 76% | 64% | 58% | <50% | N/A |
| T | 94% | N/A | 44% | 21% | N/A |
| F | 63% | 46% | 36% | N/A | N/A |

Table 1: Percent of original peel strength after 1000 hours of thermal aging.

| Flexible Copper Clad | Clad Service Temperature | UL MOT | UL RTI |
|---|---|---|---|
| A | >225 | 180 | 200 |
| X | >225 | TBD | TBD |
| D | >225 | TBD | TBD |
| L | 150 | None | 200 |
| T | 140 | TBD | 200 |
| F | >105 and <125 | 105 | 200 |
| Service Temperature is determined by the temperature where the peels are 50% of original, or better than AS spec. | | | |

Table 2: IPC service temperature rating vs. UL rating (Degrees C).

Table 2 shows the service temperature rating we have tentatively assigned for these products.

L shows higher values than some might have predicted but this rating is consistent with experience in flex applications. Clearly A has a much higher service temperature than the UL rating would suggest. The table shows that RTI ratings are not a good method of predicting service temperature. (Service temperature is mainly determined by peel strength; RTI is done on samples with no copper foil.)

When the flex clads were tested at 250°C in an air oven per the IPC service temperature test, the copper foil became so brittle that the peel strength could not be measured. Therefore, the actual service temperature of A, X, and D could be 250°C, but we have not been able to measure peel strength because of copper oxidation. A quick test to add ENIG to the copper surface proved unsuccessful because the nickel made the copper too brittle. To measure service temperature of high temperature flex clads above 225°C will require development of a new technique.

### Flexible Bondply and Coverlay Testing Results

UL does not assign a MOT rating for flexible bondplies and coverlays. In some cases, it is possible to get a MOT rating for a combined package (clad and coverlay for example). The IPC service temperature test method was adapted to test bondplies and coverlays. The bondplies and coverlays are laminated to copper to create clads and then tested as if the samples were clads.  Our testing so far has shown wide variation in service temperature ratings of bondply and coverlays, suggesting that the test

method has many issues with reproducibility. Our internal testing shows service temperature for coverlays that are well below the accepted performance in the field. This suggests that the present method does not measure the true capability of coverlays and bondplies.

Some of these issues are caused by the process of microetching sheets of copper foil, which get laminated to the coverlay or bondplies to form a clad. This obviously is not easy to process. The other issue is the coverlay sample that is aged in the oven is just coverlay with copper foil on one side. Previous testing has shown that adhesion loss between copper foil and the dielectric is driven by the presence of oxygen. The multiple layers of copper, bondply and coverlay will reduce the amount of oxygen present at the copper interface, which will prolong the life of the flex circuit at higher temperatures.

We are designing a new internal method to measure service temperature for coverlays that captures all of the possible failure modes. This method makes a simple flexible circuit with coverlay(s) laminated over circuit lines designed for bend testing. Temperature aging of these circuits should show reduced bend performance if any of the three possible failure mechanisms occur: loss of copper adhesion, loss of adhesion between dielectrics (such as clad and coverlay) or increase brittleness of the dielectrics (especially of the coverlay). The number of bends that the test circuit can survive will decrease with any of the failure modes.

The data in Table 3 shows bend performance after aging at 180°C. The copper clad laminate used for this test was an all-polyimide clad. Listed in the table are the coverlays tested. The percentages are based on the ratio of bends after 1000 hours of temperature aging to the number of bends with no aging. For this evaluation, the coverlays passed if the bend performance after thermal aging was at least 50% of bend performance with no aging.

The results show that some coverlays actually show good service temperature performance. The L coverlay has been known to survive in the temperature range of 150–180°C depending on the circuit design and environment. The bend

| Coverlay | Starting Bends AR | Starting Bends AS | 180ºC |
|---|---|---|---|
| X | 477 | 468 | 73% |
| L | 425 | 295 | 134% |
| J | 234 | 210 | 61% |
| Bend Ratio 4.5 | | | |

Table 3: Percentage of bends after thermal aging, 1000 hours.

version of the service temperature gives a much more realistic value for L than the official IPC service temperature test method for coverlays.

The J coverlay appeared to fail mainly because of brittleness, and this reduced bend performance. This confirms that brittleness is one of the possible failure modes with high-temperature aging, and this new method was able to capture the performance loss with this failure mode. This is probably also the case for the L, however, it is difficult to tell because of acrylic adhesive is covered with a polyimide film.

The all-polyimide coverlay based on experimental film, X, shows very good performance, in part because there is an all-polyimide flexible circuit containing a polyimide clad and coverlay. As long as good adhesion can be achieved between the polyimide and the copper foil, an all polyimide flexible circuit should have the best high-temperature performance.

We have developed an all-polyimide coverlay and bondply to use with the all-polyimide copper clad laminates based on the X film. The new polyimide coverlay will require lamination temperatures of around 290–300°C (554–572°F), which will limit the use to only certain fabricators. So far it is clear that this is the best approach to achieve flexible circuits that can survive high temperatures.

We will continue to refine this new coverlay service temperature test method. If it continues to show results more consistent with field experience, we will recommend that it be considered as an IPC test method.

**Summary**

To meet the increasing needs for flexible circuit materials for high-temperature applications, new test methods will need to be developed. These new methods will assign new ratings, and we believe ratings that are consistent with actual performance. The present IPC service temperature test seems to work well for testing copper clad laminates. It does not work well for bondplies and especially coverlays. We have demonstrated a new coverlay test based on bend testing. The overall results clearly show that all polyimide clads, bondplies and coverlays will provide the highest service temperature performance. **PCB**

Sidney Cox is a product development research scientist at DuPont Circuit and Packaging Materials.

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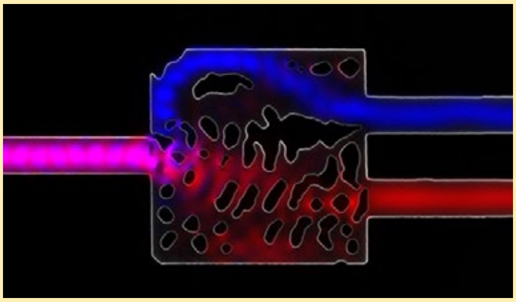
## Stanford Creates Super-efficient Light-based Computers

Stanford electrical engineer Jelena Vuckovic wants to make computers faster and more efficient by reinventing how they send data back and forth between chips, where the work is done.

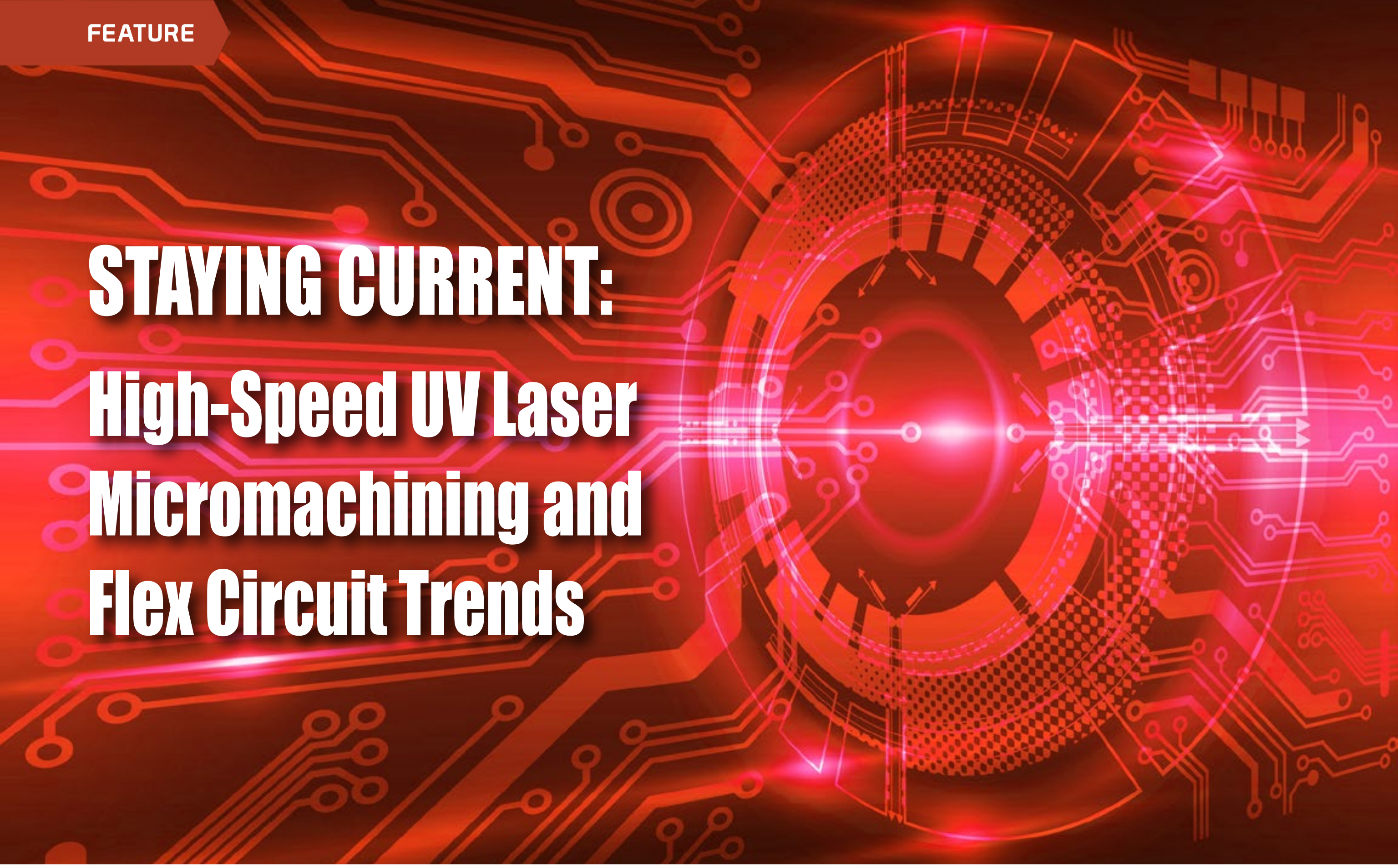
In computers today, data is pushed through wires as a stream of electrons. That takes a lot of power, which helps explain why laptops get so warm. In essence, the Stanford engineers want to miniaturize the proven technology of the Internet, which moves data by beaming photons of light through fiber optic threads.



The Stanford work relies on the well-known fact that infrared light will pass through silicon the way sunlight shines through glass.

The Stanford algorithm designs silicon structures so slender that more than 20 of them could sit side-by-side inside the diameter of a human hair. By automating the process of designing optical interconnects, they feel that they have set the stage for the next generation of even faster and far more energy-efficient computers that use light rather than electricity for internal data transport.

FEATURE



# STAYING CURRENT: High-Speed UV Laser Micromachining and Flex Circuit Trends

**by Patrick Riechel**
ESI

Consumer electronics, wearable devices, the Internet of Things, medical devices, automotive, and military electronics markets are driving flexible circuits into increasingly more products. The push for smaller, cheaper, and more capable devices in each of these industries demands flexible circuits. This can mainly be attributed to the flexible circuits' ability to alleviate some of the packaging difficulties resulting from moving to smaller devices—flexible circuits allow for more packaging flexibility, both literally and figuratively.

## Trends in Flexible Circuit Processing

In order to reduce costs while improving capabilities (generally in the form of more processing power, higher clock speeds, more sophisticated communications technologies, and lower power usage), the industry is moving to more complex board stack-ups, more complicated, smaller, and fine-featured shapes, and a higher usage of small blind and buried microvias and ever-thinner materials.

Although double-sided flexible circuits are still the most typical construction, complex multilayer stack-ups and rigid-flexible circuits are becoming more common. These multilayer constructions allow the designer to make the flexible circuit more functional. Not only do they allow for more signals to pass through the circuit and the robust placement of chips, they also enable the designer to implement electromagnetic shielding to prevent noisy high-speed signals from interfering with sensitive signals both inside and outside of the product. Another benefit is enhanced impedance control for both high-speed and RF communications signals. Multilayer constructions such as these come with unique challenges for via processing.

Given the typical use of flexible circuits to fit into small and difficult spaces and the trend toward smaller and thinner end-user devices, it is not surprising that the shapes and sizes of flexible circuits are becoming more complex, fine-featured, and smaller. These shapes and sizes are beginning to drive a need for more accurate and fine-grained cutting methods for both circuit and coverlay material.

While simple through vias are still the most common method of connecting signals from

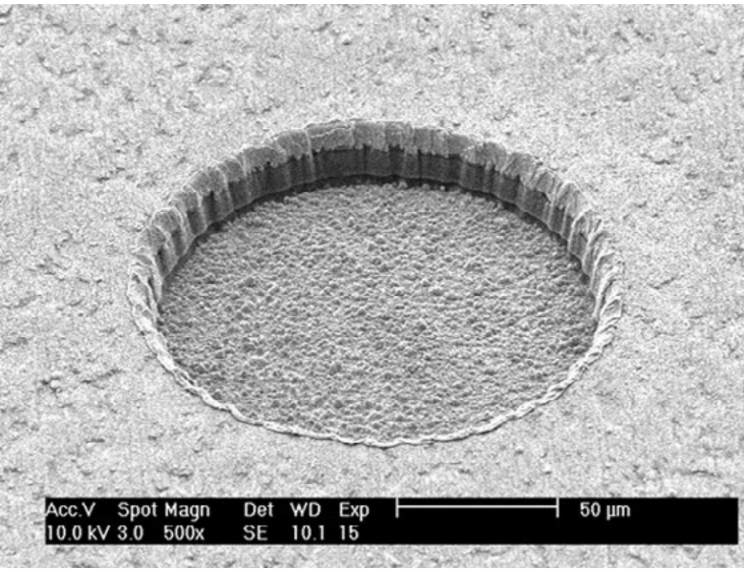



Figure 1: 150 µm blind via drilled in 5/13/5 material.

layer to layer, the push for smaller devices, better signal integrity of high speed signals, and lower capacitance to reduce parasitic power losses is driving higher usage of blind and buried microvias. Chip and circuit sizes are also shrinking, which requires smaller microvias, thinner lines and tighter spacing between signals, and higher placement accuracy to process all of these features.

While the flex circuit industry continues to use double-sided 12 µm Cu/25 µm PI/12 µm Cu copper-clad laminates, more and more manufacturers are beginning to use thinner materials such as 12/12/12 and 5/13/5 (Figure 1) copper-clad laminates in production, with some companies experimenting with novel additive technologies. For example, some suppliers are drilling unclad dielectrics and adding an extremely thin copper layer to achieve even smaller geometries at even lower costs. This trend toward increasingly thinner material drives lower material cost and higher flexibility, while increasing micromachining difficulty.

### Processing Methods and the Latest Trends

In the discussion so far, we have seen how end-user market requirements have begun to impact the use of flexible circuits as well as the complexity and difficulty of their microvia drilling and circuit cutting needs. Let us now turn to the three methods currently most frequently used to drill and cut printed circuit boards in general—mechanical processing, $CO_2$ laser processing, and UV laser processing—and explore some of the reasons why UV laser tools are uniquely suited to addressing flexible circuit processing needs as well as keeping up with the latest market trends.

While mechanical processing methods are typically the most cost-effective means of processing material, they have several issues in keeping pace with the latest trends. Die punching or routing the outlines of flexible circuits and associated coverlay material become impossible as part sizes and curve radii shrink beyond the capability of the die manufacturer or below the size of the routing tool.

Mechanical via drilling becomes excessively expensive as via sizes shrink due to the higher cost and breakage of small-diameter drill bits. Mechanical drills also suffer from lower accuracy. This is due to two factors. First, at smaller diameters, these machines suffer from “drill wander” caused by the higher length-to-diameter ratio of the drill bit. Second, typical multi-head mechanical drill benches drill the exact same locations on all panels and do not compensate for the small scaling inaccuracies and deformations that each individual panel typically suffers from. Furthermore, mechanical drilling has insufficient depth control accuracy to robustly drill blind vias in typical flex circuit constructions. Typical flexible circuit copper thicknesses are on the order of (or thinner than) the depth-control accuracy of the drilling tool. These problems will be challenging for mechanical technology to overcome as the flexible circuit roadmap progresses towards smaller circuits, higher accuracy, and smaller microvias.

$CO_2$ laser processing has found a solid place in high-volume manufacturing of relatively large vias in rigid board processing, but has several issues that have limited $CO_2$ tools from being widely used in processing flexible circuits. $CO_2$ technology is often used in blind via processing of rigid copper-clad laminates due to the fact that the $CO_2$ laser’s far infra-red wavelength (typically between 9.4 and 10.6 µm) is poorly absorbed by copper. Once the top layer of copper is removed, subsequent laser pulses used to remove the dielectric material pose effectively zero risk to damaging the bottom copper layer.

Typical industry practice to enable copper-direct drilling with $CO_2$ lasers is to pre-treat the top copper layer using a variety of special methods including black oxide, inter-granular micro-etching, and special laser direct drill (LDD) foils. This pre-treatment process adds additional cycle time and capital cost and typically enables drilling copper layers only up to approximately 12 µm. Given this limitation, $CO_2$ lasers are effectively prohibited from processing through vias in copper-clad laminates as well as L1 to L3 (and beyond) blind vias in multilayer stack-ups.

Another complication is that $CO_2$ lasers typically leave dielectric residue behind after drilling. And since the standard dielectric material in flexible circuits is polyimide and the desmear process for polyimide either requires very caustic chemicals or aggressive plasma etch processes, most manufacturers avoid $CO_2$ lasers for flexible circuit drilling. Furthermore, due to the high energies and long pulse widths involved in $CO_2$ processing, a $CO_2$-processed material generally results in significant carbonization, which must also be removed via aggressive post-processing to avoid quality and reliability issues later in the circuit lifecycle. Finally, due to the $CO_2$ laser's long wavelength, such laser systems cannot keep up with the flexible circuit industry's push to smaller and smaller via sizes.

UV laser processing overcomes many of the limitations that both mechanical and $CO_2$ laser processing face in meeting the evolving needs of the flexible circuit industry. The UV wavelength (typically around 355 nm for the most common Nd:YAG diode pumped lasers and dropping to below 200 nm for more specialized excimer lasers) has several beneficial attributes that help address these needs.

First, its wavelength is absorbed very well by most common flexible circuit materials, such as copper, polyimide, and various adhesives and resins. This enables UV laser micromachining to be extremely versatile – processing blind and through vias through thick and thin copper-clad laminates, unclad materials, and multilayer stack-ups without any costly and often toxic pre-treatment steps. An example of a multilayer through via is shown in Figure 2. UV laser tools also can be used to remove layers of copper, excess adhesive, and improperly placed coverlay material, as well as excising complex and fine-featured shapes of circuits and coverlay material.

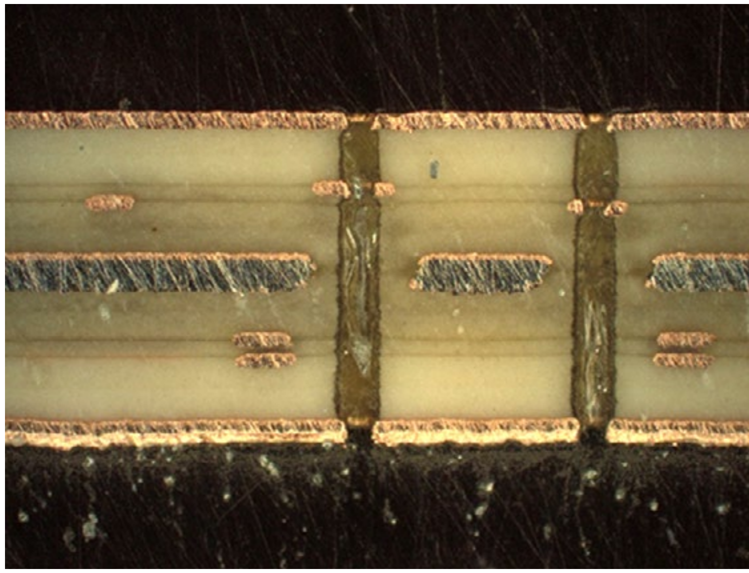


Figure 2: Through-vias drilled by UV laser in a multilayer stack-up.

Another benefit of using UV lasers is that most smear and carbonization can be avoided when drilling vias and cutting circuits. As such, much less aggressive desmear or other post-processing steps are needed before plating (if drilling) or reliability testing (if excising the panels). Given UV's short wavelength, typical focused laser beam "spot sizes" are in the 15–25 µm range. That means that with precise beam positioning, features sizes can range from the size of the entire processing area down to that 15–25 µm spot size.

Finally, with proper precision engineering techniques, a UV laser tool can achieve extremely accurate placement of vias and other features. At this time, the most typical tool accuracy specification is ±20 µm, although specialty shops can and do achieve better than ±10 µm with that same tool by maintaining tight control over the tool's and the processing materials' temperature and humidity, as well as enforcing strict alignment, calibration, and pre- and post-processing procedures.

## Understanding UV Laser Micromachining Tools

Beyond having the capability of processing a flexible circuit to customer specifications, the most important factor in deciding on a production tool is cost of ownership. Cost of ownership means different things to different board shops.

For high-volume board shops, cost of ownership will typically mean cost per panel over the course of the system lifespan, taking into consideration upfront and maintenance costs, as well as tool productivity, part yield, and system uptime. For quick-turn shops or specialty research institutes, cost of ownership will be more influenced by how flexible the tool is in processing many different types of materials and features as well as how easy and fast it is to develop new processes for new applications. In order to achieve the best cost of ownership, UV laser micromachining tools—supported by the supplier's service and applications engineering organization—must both incorporate the most optimal laser for the end-user's application as well as be able to harness the full capabilities of the lasers.

Micromachining with lasers operates by laser ablation, whereby material is removed by an absorptive interaction between laser photons and the material being machined when the laser fluence (energy per unit area) exceeds the material's ablation threshold. The characteristics of most UV lasers—small spot size, excellent absorption in most flexible circuit materials, and relatively high pulse repetition rate (number of laser pulses per unit time)—require precise energy dosing and fast and accurate beam positioning to fully take advantage of their capabilities. That becomes even truer given industry trends to thinner materials and smaller vias with increasing accuracy requirements.

Precise and well-distributed energy dosing is very important as shown in Figures 3 and 4 to reduce or avoid quality issues such as damage to the bottom copper layer and adhesive or polyimide residue in blind vias, etch back of via sidewalls, fiber protrusion in rigid-flex constructions, and copper splash, to name a few.

Especially with the trend toward materials with thinner copper foils, precise power control is extremely important to avoid yield issues. The drill tool must employ methods that keep laser transients from reaching the material to ensure consistent process quality. Since typical via sizes are larger than the UV laser spot size, consistent beam positioning with flexible motion paths (e.g., spirals, circles, etc.) must be available for robust process development. For multi-revolution processes, pulse distribution methods should be used to avoid localized ablation.

Fast and accurate beam positioning is equally important to avoid quality issues, while also

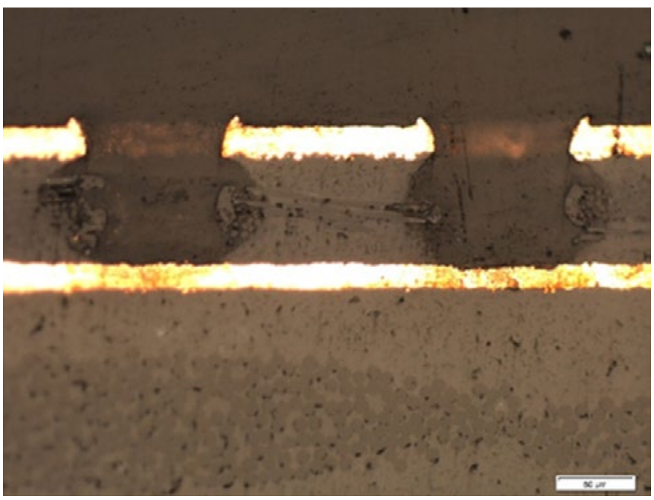


Figure 3: Poor etchback and fiber protrusion with poor energy dosing.

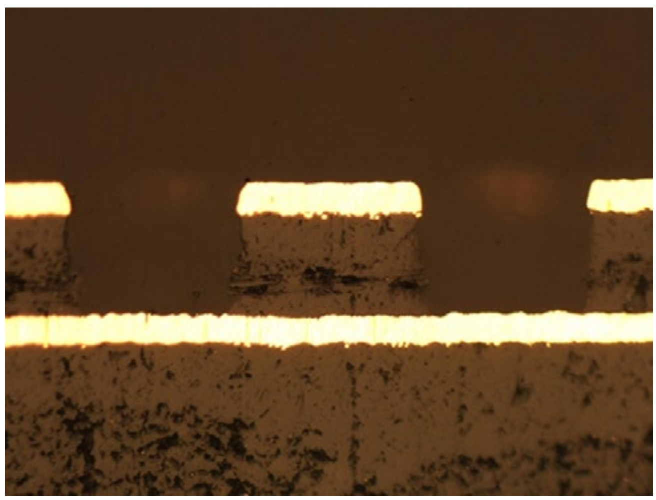


Figure 4: Minimal etch back and fiber protrusion with good energy dosing.

ensuring maximum productivity. A must-have for any UV laser micromachining tool is a telecentric lens. As shown in Figure 5, a telecentric lens ensures that the laser beam always strikes the material at a 90-degree angle, thereby creating a perpendicular via or cut anywhere the machine processes the material.

Typical UV laser tools use a combination of linear stages and galvanometers (motorized mirrors) to position the laser beam on the part being processed. Many manufacturers use a move-then-process method to cut the full panel area—moving the stage to an area on the panel within the galvanometer field, processing that area, stopping the laser, moving to the next area, processing, stopping, etc. This results in a lot of non-value-add time since the laser is off during each long move. In addition, due to small galvanometer and linear stage errors, as well as due to optics aberrations, that method can result in incongruous cut lines where one galvanometer field touches the next.

The method of compound beam positioning resolves both of these issues by moving all beam positioning devices at the same time in a manner similar to hand-writing. For a stage-plus-galvanometer beam positioning system, one can think of the stage as the arm making the large and slow motions to cover the entire page at the same time as the galvanometer acts as the wrist and hand, making the small, precise, and fast motions to form the words. This method ensures high productivity given that very little time is wasted with the laser not processing, as well as avoiding quality problems caused by galvo field incongruities since the laser is continuously processing while moving.

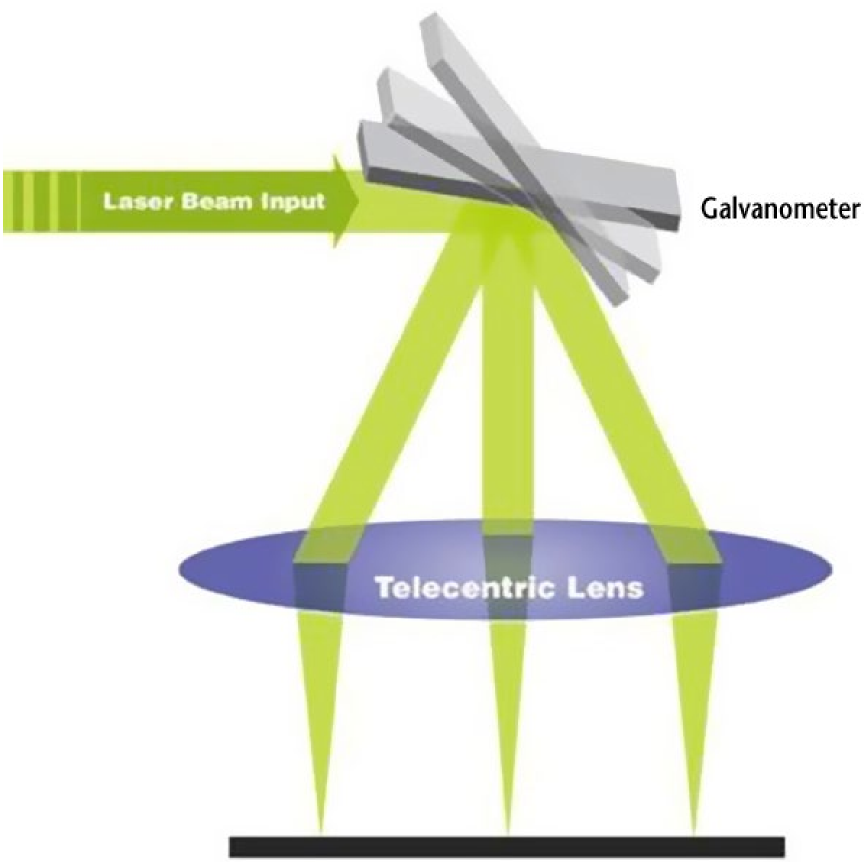



Figure 5: A telecentric lens restores the laser beam to vertical no matter the galvanometer angle.

### Accurate High-Speed Beam Positioning

Precise beam positioning at high velocities is more difficult. It is crucial to maintain adherence to part dimensional tolerances, as well as to avoid localized heating quality issues by moving the beam fast enough to spread out laser pulses even at high laser pulse repetition rates. Accurate high-speed beam positioning becomes also becomes important as feature sizes shrink, and thinner and more heat-sensitive materials are used.

Here, good tools set themselves apart. It becomes much more difficult to maintain precise beam positioning at high velocities for small features and tight curves given the high accelerations that the beam positioning components must overcome. One method of overcoming these challenges is to include a solid-state device as part of the beam positioning mechanism since such solid-state devices have effectively zero inertia. ESI's Third Dynamics™ patented beam positioning technology is one such example. By coupling a first level of linear stage motion with a second level of galvanometer (motorized mirrors) motion, as well as a third level of solid-state device motion, it is possible to achieve well-placed laser pulses at very high beam velocities, even when processing vias as small as 25 µm as well as right-angled features.

Accuracy not only is achieved through precise beam positioning, but also through panel scaling and warping compensation. Given that materials and drilling systems expand, contract, and otherwise warp due to thermal and humidity fluctuations, post-etch relaxation, roll-to-roll handler tension, and other factors, achieving high accuracy relative to existing features requires alignment to those same features and calculated adjustments to the drill locations to compensate for those factors. With good alignment between upstream and downstream processes, it is possible to enable tighter part tolerances as well as reduce the size of via landing pads.

Achieving the best tool cost of ownership involves finding the fastest process that consistently meets the given application's quality specifications, reducing non-value-add time during which the laser is not processing, as well as reducing the system's maintenance costs.

### Laser-Material Interaction

In order to find the fastest process to meet quality specifications, a flexible circuit manufacturer must understand the basics of laser-material interaction and ideally also the latest techniques for processing a specific application. A good UV laser tool supplier will have a knowledgeable applications engineering team available to help teach these methods and provide advice on how to optimize the processes for the given application requirements and tool capabilities. Furthermore, the tool itself should have features that facilitate easy process development for rapid deployment of new processes and log process changes for quality control.

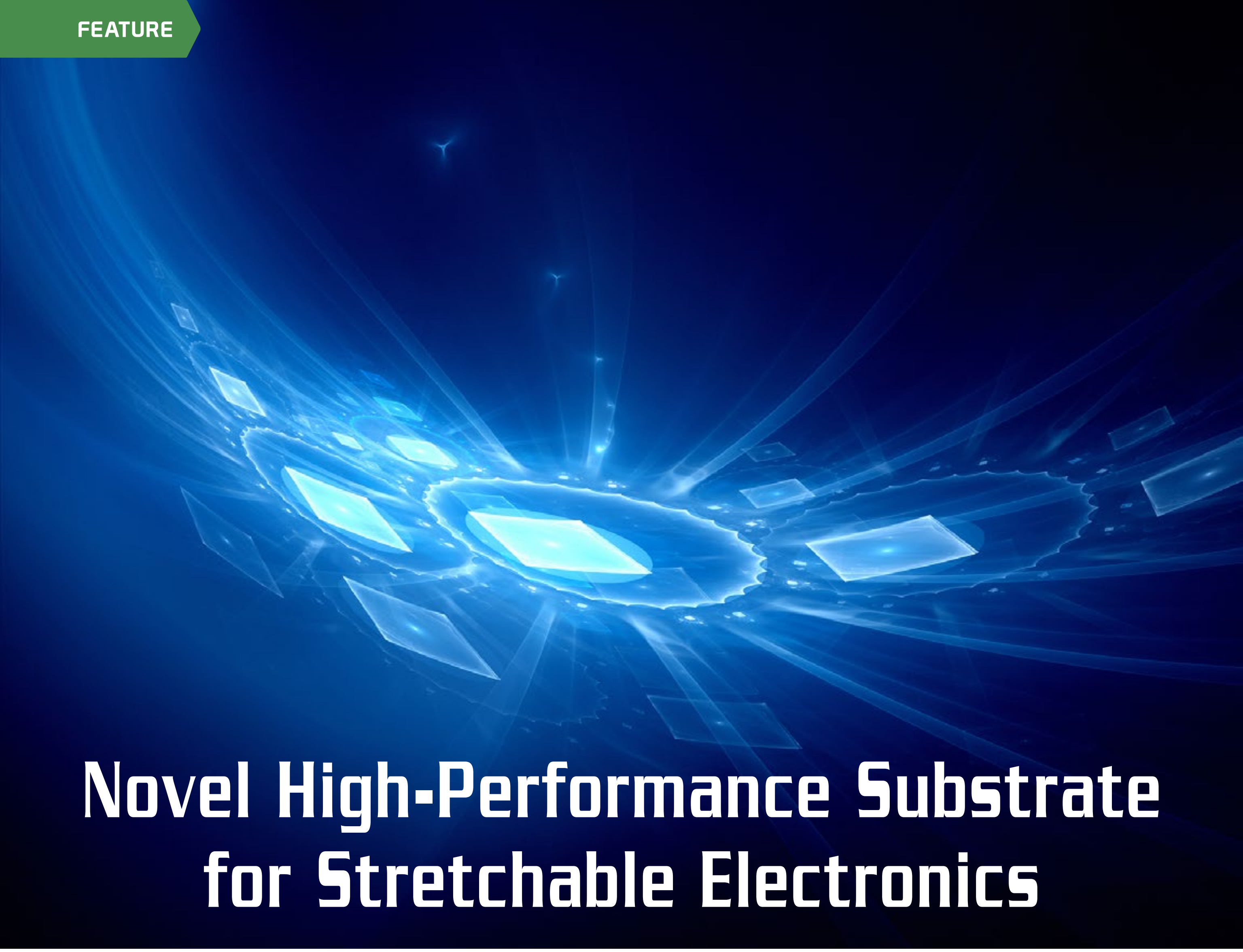
Non-value-add time can be reduced in a number of ways. Automation, whether through roll-to-roll handlers for high volume flexible circuit manufacturing or through stack handlers for medium-volume manufacturing, can reduce operator error and speed up loading and unloading procedures. Automated vision alignment routines are another way to reduce operator involvement and speed up alignment time. Good debris removal and optics protection mechanisms can reduce both preventive maintenance and unexpected maintenance procedures and minimize laser and optics consumption to reduce maintenance costs.

Maintenance costs and system downtime can also be reduced when the supplier has well-trained service support teams for preventive maintenance and troubleshooting support. On-system logging and diagnostics features aid rapid turnaround of fixes with targeted solutions (rather than the alternative approach of replacing parts to see what fixes the problem). Finally, given that the laser will be one of the highest-cost consumables, the supplier should have chosen a reliable laser to help achieve the lowest possible cost of ownership over the course of the system lifespan.

### Summary

Specific market trends are driving increasingly more flexible circuit usage, as well as more difficult-to-process materials and features. We have evaluated three different methods—mechanical, $CO_2$, and UV laser processing—on how well they can meet the evolving needs of the flexible circuit market and demonstrated that UV laser processing is best-equipped of those three. Finally, we explored some of the most important factors to consider when choosing a UV laser processing tool. This is an exciting and evolving time for the electronics industry and flex circuit manufacturers. Make the most of it: Reach out to various UV laser micromachining system vendors and educate yourself on what you might be able to achieve. **PCB**

Patrick Riechel, MSc MBA, is product manager for flexible circuit micromachining tools at ESI.



# Novel High-Performance Substrate for Stretchable Electronics

**by Shingo Yoshioka, Tomoaki Sawada and Takatoshi Abe**
PANASONIC CORPORATION

Stretchable circuits are an evolving branch of electronics interconnection technology and the subject of growing interest to product developers seeking to provide novel wearable electronic solutions for consumer and medical markets. Such circuits are designed and manufactured using resilient materials which allow them to expand and contract with the movements of the user or to conform to nonplanar surfaces making possible a wide range of innovative and fanciful electronic interconnection devices. Obviously, the material used is a key element in making a stretchable circuit. There are a range of different types of thermoplastic polymers available in film form that can be effectively stretched; however, once stretched beyond their elastic limit the material deforms to a new length greater than that which was designed. There are as well elastomeric materials, such as urethanes, which have seen use in the manufacture of circuits which can be stretched and return to their original length. These materials tend to be opaque, which limits the scope of possibility for their use. A new transparent, high-performance thermal setting stretchable material could open doors to a range of new and innovative products.

## New Stretchable Material Characteristics

The new material is capable of stretching to 150% of the original length without hysteresis. Figure 1 provides a comparison of stress-strain plots of the new material compared with thermoplastic PEN.

Another key attribute of the material is its ability to reliably return to the original length

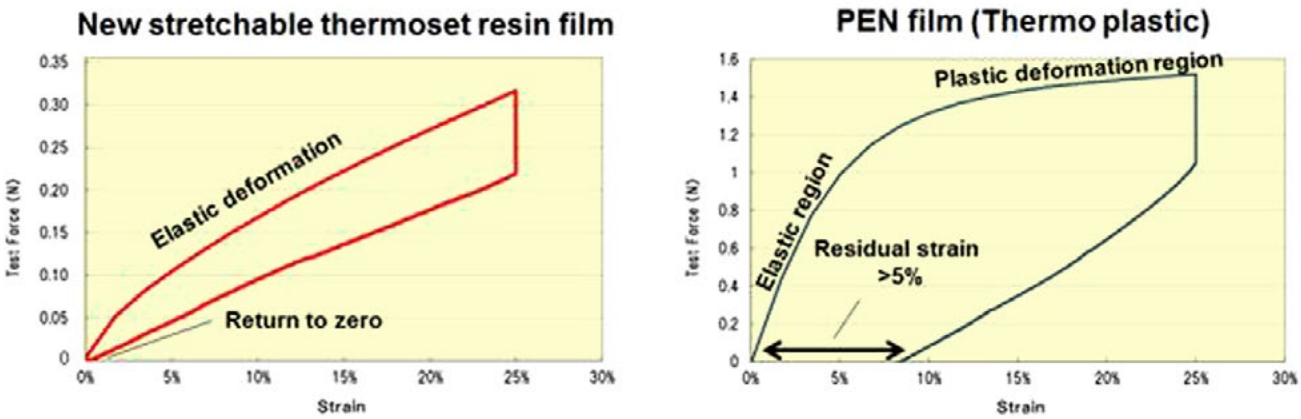



Figure 1: A cornerstone feature of any viable stretchable material is its ability to return to zero after stretching as shown on the left. As can be seen in the right-hand image, thermoplastic materials have a very limited range of elasticity, severely limiting its use in stretchable applications and beyond which the material plastically deforms.

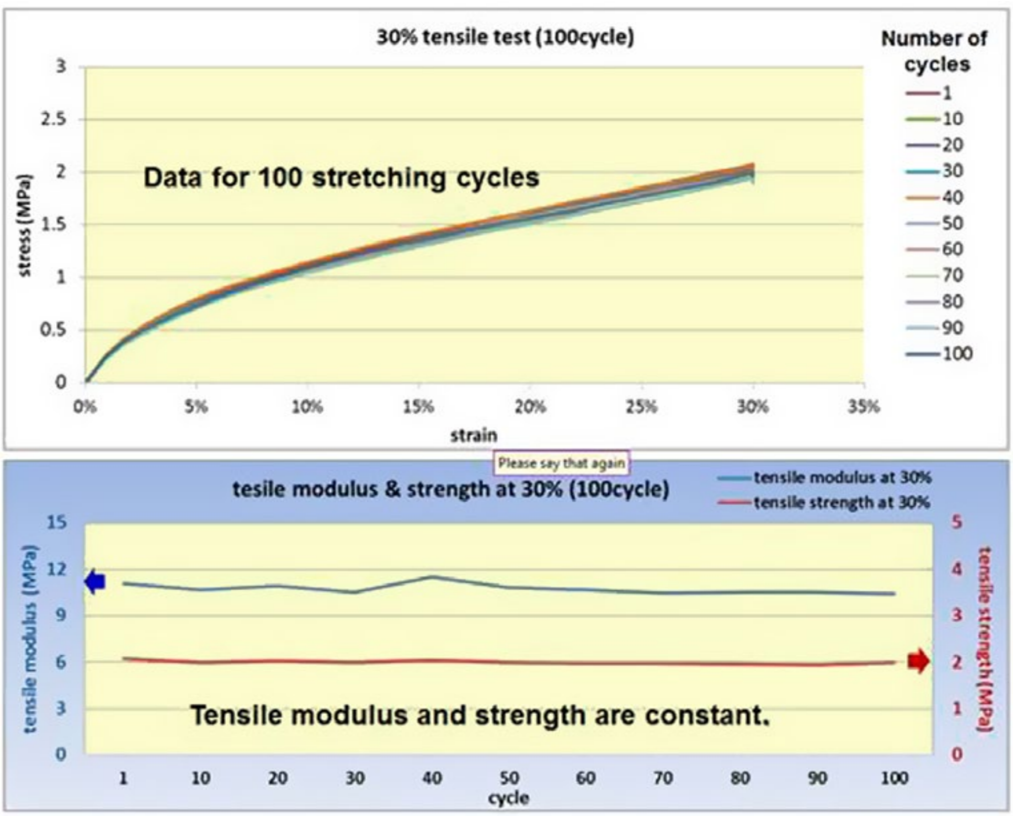



Figure 2: Consistency in material performance over multiple cycles of stretching is an important feature of the new material.

even when stretched numerous times, as will likely be required in numerous future applications. The new material excels in this regard, shown in Figure 2.

The mechanical and thermal properties of the new material are superior in many impor-

| Item | Test method | unit | New Stretchable Thermoset Resin | PEN (Thermoplastic) |
|---|---|---|---|---|
| Tensile Modulus | ASTM D882 | MPa | 11 | 6000 |
| Tensile Strength | ASTM D882 | MPa | 10 | 260 |
| Elongation at break | ASTM D882 | % | 170 | 100 |
| Yield point | ASTM D882 | % | None | 5 |
| Stress relaxation | @50% elongation | % | 67 | 28 |
| Melting point | - | ℃ | None | 262 |
| Water Absorption | ASTM D570 (D-24/23) | % | 0.4 | 0.3 |
| Adhesion to Cu foil | @23℃30% | kgf/cm | 1.5 | 1.1 |
| Adhesion to FR-4 | @23℃30% | kgf/cm | 1.0 | N.A. |
| Resistivity | ASTM D257 | Ω·cm | $2 \times 10^{15}$ | $1 \times 10^{15}$ |

Measured values.

Figure 3: A comparison of the material properties of the new stretchable thermosetting resin and PEN.

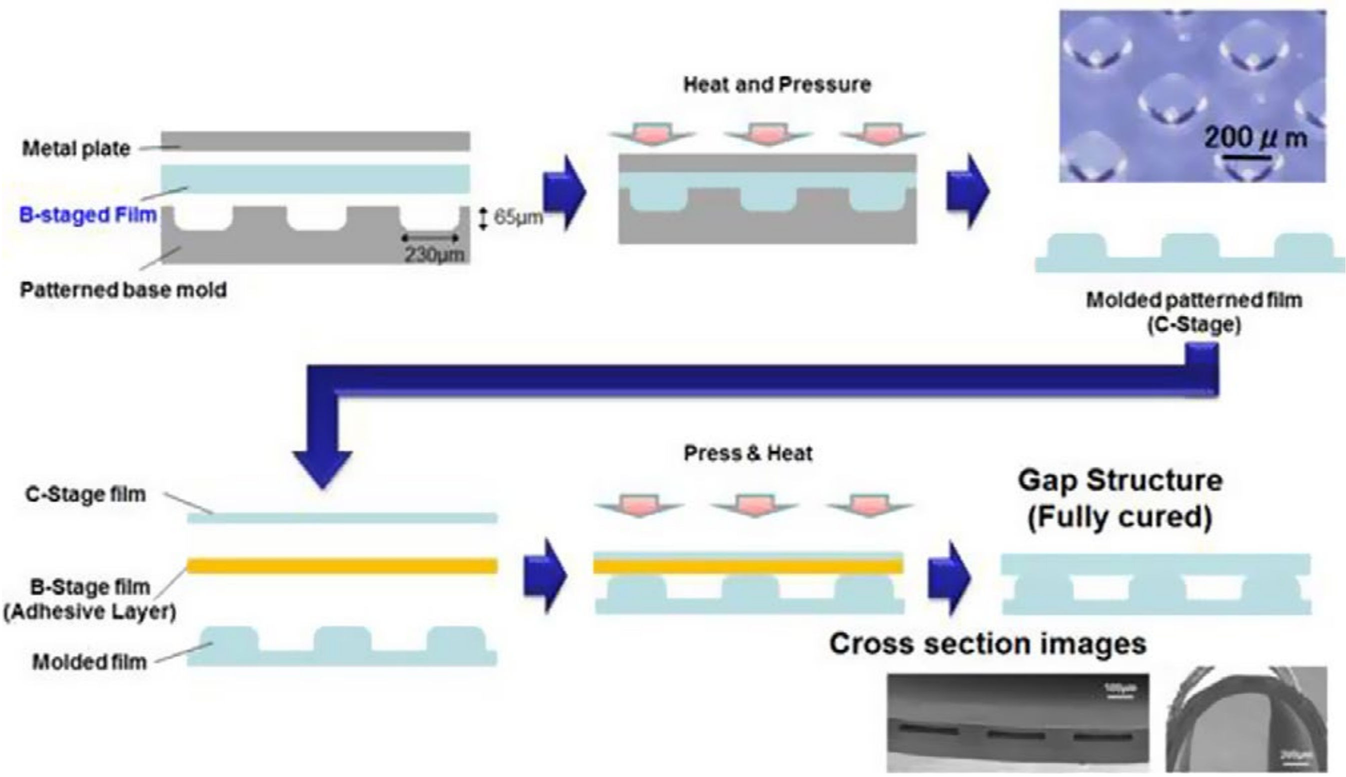



Figure 4: Process steps for making an air gap laminate and photomicrographs of the material both before and after lamination.


Figure 5: In comparison with ITO, the new conductive material which has been formulated offers superior performance.

tant areas including total elongation and adhesion both to copper foil and FR-4 laminate. It is also unique in that is has no melt point making it amenable to soldering with higher temperature lead free solders. A comparison of the new material with PEN is provided in Figure 3.

Because the material is thermosetting, it opens up possibilities to make a wide range of new and unique structures with limits that are defined only by the creativity of the designer and abilities of tool maker. To stimulate the reader's thinking relative to new possibilities, Figure 4 shows an example of a process for structure having an air gap between layers of the material held apart by molding an array of miniature posts into the material and then laminating a sheet of cured material to the molded sheet using a sheet of B-staged material.

### Stretchable Conductor Material: A Natural Companion

In addition to the stretchable base material, an equally novel conductive material has been developed as a natural companion, which is suitable for use in display and sensor products near term and possibly others in the not too distant future. The thin (0.1 µm) conductive coating material is 85% transparent and nominally 300 Ohms/square can be stretched reliably to greater than 10% of original length. As shown in Figure 5, the performance is superior to indium tin oxide (ITO) coatings which are brittle and easily fracture.

### Summary

A high-performance stretchable substrate such as the one described here offers both new levels of performance and unique processing options, which could increase the material's appeal. In tandem with the companion high-transparency conductive layer, design options and opportunities are further expanded. **PCB**

Shingo Yoshioka is the general manager at the Technology Development Center, Electronic Materials Business Unit of Panasonic Corporation.

Tomoaki Sawada and Takatoshi Abe are staff engineers at Technology Development Center, Electronic Materials Business Unit of Panasonic Corporation. For more information, click here.

## Ford Opens IP Portfolio to Fuel EV Industry Growth

Ford Motor Company is offering competitors access to its electrified vehicle technology patents – a move to help accelerate industry-wide research and development of electrified vehicles.

In 2014, Ford filed more than 400 patents dedicated to electrified vehicle technologies. This is more than 20% of the patents the company filed – totaling more than 2,000 applications.

To access Ford's patents and published patent applications, interested parties can contact the company's technology commercialization and licensing office, or work through AutoHarvest, an automaker collaborative innovation and licensing marketplace. AutoHarvest allows members to showcase capabilities and technologies, then privately connect with fellow inventors to explore technology and business development opportunities of mutual interest. The patents would be available for a fee.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# Electronics Industry News
## Market Highlights

### Commercial Avionics Systems Market Driven by Modernization

According to a new market research report "Commercial Avionics Systems Market by Sub-segment, by Platform (fixed wing and rotary wing), and by Geography—Forecast 2014–2020," published by MarketsandMarkets, the commercial avionics systems market was estimated at $15,748.26 million in 2014, at a high CAGR of 7.06% from 2014–2020, to reach $23,715.24 million by 2020.

### Smart Home Automation System Market to Reach $34B in 2020

Global revenues from smart home automation systems will grow at a 21% CAGR between 2015 and 2020, according to ABI Research, with North America accounting for the lion's share of the market, followed by Europe and Asia-Pacific.

### PC Shipments in EMEA Decline amid Currency Fluctuations

PC shipments in Europe, the Middle East, and Africa (EMEA) reached 20.2 million units in the first quarter of 2015—a 7.7% decrease year on year, according to International Data Corporation (IDC). After a strong 2014, the market returned to a decline as expected, with business renewals decelerating after last year's uplift prompted by the end of Windows XP support.

### Tablet Market Experiences Contraction amid Competition

Worldwide tablet shipments recorded a year-over-year decline for the second consecutive quarter in the first quarter of 2015 (1Q15). Overall shipments for tablets and 2-in-1 devices fell to 47.1 million in 1Q15, a -5.9% decline from the same quarter a year ago, according to preliminary data from the International Data Corporation (IDC) Worldwide Quarterly Tablet Tracker.

### Automotive Powertrain IC Market Up 8.3% in 2014

IHS Technology forecasts that revenues related to powertrain semiconductors will increase with a compound annual growth rate (CAGR) of nearly 6% in the next five years, from $7.2 billion in 2014 to $9.5 billion in 2019.

### IoT Adoption in India will Advance at a Slow Pace Through 2020

Indian enterprises are at the early stages of understanding the impact of the Internet of Things (IoT) on their business, according to Gartner Inc. While the concept of IoT is not completely foreign to Indian enterprises, adoption will advance slowly through 2020.

### In-Building Wireless Market to Reach $9B by 2020

ABI Research's latest in-building wireless market data forecasts that North America will drive the overall market while Europe and Asia-Pacific will pick up the pace during 2016. The market for in-building wireless equipment and deployments will more than double the current market by 2020.

### TrendForce: More Worries than Hope in Q2 Panel Market

The prices for TV panels of mainstream sizes will hold steady in April as Chinese brand vendors are stocking up for Chinese Labor Day sales, according to WitsView.

### Wearable Technology Market Forecast 2015–2020

The global wearable technology market has thus far not quite delivered upon previous expectations of revenues, consumer adoption and even technological advances. However, 2015 might be the breakthrough year in which wearables begin to achieve that mass market acceptance that has long been expected.

### Wi-Fi Equipment Market to Recover

The worldwide consumer wi-fi equipment market increased 5% in 2014, surpassing 166.1 million unit shipments. "Shipments of devices which support the 802.11ac standard grew significantly in 2014, representing more than 11% of total access point shipments," said Jake Saunders, VP and practice director, ABI Research.

# Flex and Rigid-Flex Circuit Testing: Challenges & Solutions

**by Todd Kolmodin**
GARDIEN SERVICES USA

Although flex circuits are nothing new in today's technology roadmap, the testing of unpopulated flexible circuits can be challenging. These circuits can be very thin, have challenging geometrical configurations and in some cases be a combination of rigid bare board and flex. There are basically three different methods available to test these challenging circuits: manual, fixture and flying probe.

## Manual Test

Manual testing simply involves a digital volt meter (DVM) where the circuits are "rang out" by testing the continuity (opens) and discontinuity (shorts) of the individual nets. However many semi-affordable DVMs can only provide continuity measurements true to the IPC and MIL specifications as the resistance resolution for discontinuity (shorts) testing cannot test to the isolation requirements of the specifications.

## Fixture Test

Flex circuits, in many cases, can be tested by the use of both dedicated (wired) and universal grid (pinned) fixtures. Both of these fixtures are desired when high volume is manufactured. However, the challenge is registering the product to the actual fixture. Some, but not all, flex circuits have mounting holes that can be used to register the circuit to the fixture, which makes the use of fixtures optimal for high volume. Unfortunately, mounting holes may be non-plated and the repeatability of registration may be compromised. In other cases, there may be no mounting holes at all as the flex circuit is "clamped" to a connector, making fixture registration difficult. To overcome the challenge, "dams" or registration barriers may be designed into the fixtures so that the flex circuit may still repeatedly register to the fixture. This can be extremely difficult as many current flex circuits have extremely tight designs and very small landing pads (lans.) Mis-registration on these very small pads can result in "mouse biting" or full destruction of the pad itself, resulting in scrap.

## Flying Probe Test

This method can be the most advantageous option for testing low to medium volumes. The first advantage is of course cost. The fixture is eliminated as well as the time taken to build it. With only front-end programming required, this is an excellent option for prototypes and

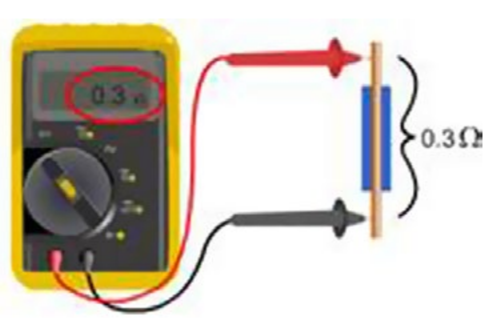


Figure 1: Standard DVM probe test.

Figure 2: Fixture with dams.

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small to medium batches. The newer flying probes have some advantages over fixtures:

- Registration holes are not required for alignment
- Pad sizes down to .003" can be tested successfully without the mis-registration and damage a fixture could induce
- Machines can compensate for minor mis-registration by the use of multiple fiducials, adjusting test point hit location and enhanced localized area registration algorithms.

The use of stretch frames comes in to play here and is a great advantage. The circuit is placed in the clamping system of the machine and then is stretched tight to provide the robust contact area as a rigid board. The circuit can then be tested either single or double sided. Another option if only single sided and a complex geometrical layout the circuit can be attached to a rigid plate and then placed into the machine and tested. As noted earlier, the system can also compensate for minor misregistration by adjusting test point targeting. Another advantage that circuits with embedded passives such as resistor cores can be reliably tested. The only real disadvantage in this method is time. However with the time and cost required to build some of todays' flex and rigid-flex circuits the tradeoff of time vs reliable/repeatable and damage free results is a small price to pay.

Flex technology can only get more advanced. Airline manufacturers and military have been using flex for a long time, and increasingly, by the automoive industry—so it is not going anywhere. Testing flex is a challenge, but today's equipment is highly suitable to combat this challenge. **PCB**

Todd Kolmodin is the vice president of quality for Gardien Services USA.

VIDEO INTERVIEW

## IPC Standard 6013 Heading to Revision D

***by Real Time with...***
***IPC APEX EXPO 2015***

Guest Editor Dick Crowe and Nick Koop, Senior Application Engineer at TTM Technologies, discuss the latest revision of the flex-rigid/flex standard that is underway. The flex-rigid/flex circuit industry is booming and in many cases North America is the preferred area for manufacture.


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# PCB007 Supplier/New Product Highlights

**Growing Their Portfolio: Camtek's One-Stop-Shop in Functional Inkjet Technology**
I-Connect007 Publisher Barry Matties caught up with Dr. Boaz Nitzan, VP of functional inkjet technologies at Camtek, and the two discussed the company's expanding portfolio into inkjet printing system for PCB solder mask & legend. The new system is designed to replace conventional coating, drying, exposure and development processes currently used in PCB manufacturing.

**Insulectro Alliance with Freedom CAD**
Ken Parent, vice president of sales at Insulectro, recently sat down with I-Connect007 Publisher Barry Matties for a quick chat about the strategic alliance that Insulectro is pursuing with Freedom CAD. Parent explains how this new strategic effort is working, and what it means for customers—and OEMs.

**Rogers' Printed Circuit Materials Segment Posts Growth in Q1**
For the first quarter of 2015 net sales were $165.1 million with net earnings of $0.72 per diluted share. Arlon contributed $20.2 million of net sales and earnings of $0.17 per diluted share for the quarter.

**Circuit Foil Assigns Advanced Copper Foil Inc. as Exclusive NA Distributor for the PCB Supply Chain**
Advanced Copper Foil Inc. (ACF) is a company dedicated to the supply of high performance copper foils to North America. By announcing their newly acquired exclusive distribution agreement for the PCB supply chain with Circuit Foil Luxembourg, ACF will begin immediately to provide value-added copper foil to all regions of the United States and Canada.

**RBP Appoints Mike Carano New VP Technology and Business Development**
RBP Chemical Technology announced today the appointment of Michael Carano as vice president of technology and business development. In this role, Carano will lead RBP's product and business development activities in the electronics, medical, and mining industries worldwide.

**First EIE SA Signs New Rep Agreement for Europe with CCI EUROLAM**
First EIE SA, Geneva Switzerland, is proud to announce the signing of CCI EUROLAM as its new representative for Germany, United Kingdom and its subsidiary CTS for France.

**Technica USA Expands Partnership with Wise into Midwest**
Frank Medina, president of Technica USA, announced recently that the company entered into an agreement with Wise s.r.l. of Parma, Italy, to promote their full line of products in the Midwest of the U.S.

**Orbotech Starts 2015 with Strong Q1 Results**
Commenting on the results, Asher Levy, CEO, said: "We have begun 2015 with strong revenues, profitability and cash generation. Our larger scale of operations, as well as our enhanced diversification across businesses, end markets, products and customers, has enabled us to exceed most of the revenue and profitability targets we had set ourselves for the quarter."

**Enthone Intros AUTRONEX ICN-1000 Nickel-hardened Gold Process**
AUTRONEX ICN-1000 nickel-hardened gold process has been introduced by Enthone. The high efficiency process is production-proven to significantly reduce gold consumption, while preventing gold bleed out in low-current density areas.

**OM Group Electronic Chemicals Appoints Dr. Anson Zhang**
Dr. Anson Zhang has been appointed general manager for Asia PCB, replacing Kim Liao, who is retiring this month after 37 years of service. Dr. Anson Zhang earned his Ph.D. in chemistry from Xiamen University, China and spent the last 15 years working in various capacities for DOW Chemical Company, most recently as global business development director.

# The Flex-to-Fit Approach

**by Tara Dunn**
OMNI PCB

The flex-to-fit concept reminds us that creativity and engineering go hand-in-hand. Imagine this scenario: As an engineer, you have been tasked with the challenge of adding sensors to the front spoiler lip of the new 2015 Porsche Cayman. There is limited space available and the cavity is thin enough that running even a small wire bundle would be difficult. What do you do? Let's take a look at the flex-to-fit concept.

When there is not ample space for a conventional approach, this process, which is the convergence of the mechanical world and the electronics world, results in the ability to design a flexible circuit along the contour of an existing, irregularly-shaped structure. By taking the mechanical part, extruding the surface and then conforming to that surface, a flex circuit can be created that will fit perfectly within the confines of a limited space or cavity. In a recent conversation with Mike Brown, of Interconnect Design Solutions, he helped to clarify this process, and we discussed several exciting applications. He also explained the benefits to the flexible circuit design process.

Most electronic systems require an enclosure to support a rigid PCB. Looking beyond the constraints of an enclosure and incorporating flexible circuits within the contours of other existing structures, opens up endless possibilities. In the example of the Porsche Cayman, imagine this solution: The valence of the front spoiler lip is mechanically digitized and recreated in a 3D MCAD model. The surface is then lifted and flattened into a mechani-


Figure 1: Front spoiler lip for the 2015 Porsche Cayman. The flexible circuit can now be contoured to fit the inside cavity of the organic shape.

cal piece and translated to the ECAD environment to layout the flexible circuit. The flexible circuit is then designed to conform to the exact contour of this irregular shape. Sensors running along the flex circuit solve this challenge of limited space with the added benefit of reducing the weight.

We are in a time of amazing developments in our electronics products. Today's electronics are increasingly smaller, faster, lower power, lighter weight and feature rich. Flexible circuits are commonly used to replace wire bundles to reduce size, weight and power (SWaP). It is also common to use a flexible circuit when space is confined and circuitry is needed to be folded around corners and into tighter packaging. When traditional solutions no longer meet design constraints, the flex-to-fit model allows us an alternative path forward. As we step back and look at the existing structures available with a creative eye, it can be both exciting and a bit daunting. Imagination and analytics often compete and the combination of both is needed to determine how a space can be best utilized.

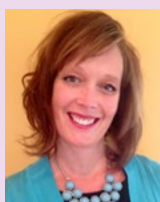
Extruding the surface of irregular shapes and creating a perfectly fit flexible circuit to integrate into the contour of that structure opens up so many possibilities. Creative thinking can save space, weight, cost and promote ease of assembly. The applications for this approach are endless. For any product in the automotive, aerospace, military and commercial sectors, where restricted weight and space are major factors, flex-to-fit offers excellent solutions.

Imagine another example: If you were to extrude the internal surface structure of a wing or fuselage of a drone or autonomous vehicle, the flex circuit could be modeled to fit the exact contour of the area it is to occupy. The cavity that would otherwise be consumed by bulky wiring cables could be made free to accommodate more features, whether it be additional sensors, monitoring or enhanced functionality.

One last example is a product that is hot in today's market—wearable electronics. Rather than run a bunch of wires and all of the sensors in a shirt, which can be a bit bulky, one possibility is to sew in flex circuits that have been modeled or molded around the human body. The flex can be sewn between the layers of material resulting in a smoother surface more closely resembling regular clothing.

While talking with Mike, it was easy to see the possibilities and the benefits to the end product. It is also important to discuss the benefits of this process to the flexible circuit design itself. By extracting the exact contour of the part, flattening it, and transferring this to the ECAD design tools, the designer is able to accurately analyze the flexible circuit design in the ECAD model. Often when using a flexible circuit in an unusually shaped area, the added length required and bend areas are difficult to determine. This approach allows the designer to perfectly fit the flex to the structure it will be aligned with. The designer is also able to accurately analyze the proper bend radius and make adjustments to remove copper layers or adhesive layers to meet standard design rules. Stiffeners and cut-out areas are also able to be analyzed directly in the ECAD system. Because all of these items can be reviewed to the exact fit of the piece, the end result is a more accurate design. There will be no surprises as the piece is assembled in the unit, which can potentially reduce the number of revisions during the design cycle.

To identify a structure that is not being utilized, digitally scribe that structure to create a MCAD model, flatten the surface of that model, and transfer that to the ECAD system for flex circuit design; this clearly demonstrates the convergence of the mechanical world with the electrical world. The convergence of these two disciplines brings so many new opportunities for today's electronics. Applications for the flex-to-fit concept are really only limited by our creativity and imagination. It is an exciting time to be involved in the world of flexible circuit design and manufacturing. **PCB**



Tara Dunn is the president of Omni PCB, which offers engineering support for technology ranging from standard boards to high-end HDI products, including sub 1-mil line and space, and stacked microvias. Dunn has more than 15 years experience in the PCB sector of the electronics industry. Her column, Flex Talk, will be appearing regularly in the Flex007 Weekly Newsletter. To contact Dunn, click here.

# Mil/Aero007 Highlights

## Stretchable Inks: Changing the Wearables Market and the Landscape of Manufacturing

I-Connect007 Publisher Barry Matties and DuPont's Steven Willoughby and Michael Burrows spoke recently and discussed a new material for wearable electronics: stretchable inks. Wearable electronics is a fast growing sector of the electronics industry that is inspiring new and exciting products, as well as changing the requirements for becoming an electronics manufacturer.

## American Standard Circuits Attains UL Approval for Isola's I-Tera Laminate and Prepreg Family

American Standard Circuits has obtained UL approval for the I-Tera laminate and prepreg family, which includes I-Tera MT, a very low-loss laminate engineered for high-speed digital applications made by Isola.

## OM Group Satisfied with Q1 Financial Results

"The year started off as planned and first quarter results are in line with our expectations," said Joe Scaminace, chairman and CEO of OM Group. "We are making progress on our enterprise initiatives and fully expect to see benefits from these actions ramp up beginning later this year."

## Innovative Circuits Installs New WISE Clean Line

Innovative Circuits, of Alpharetta, Georgia, recently installed a new Wise clean line.  The Chemstar chemistry clean line will be used for surface treatment preparation of inner-layer and outer-layer panels before dry film lamination and soldermask coating.

## Isola's Astra MT Materials Successfully Evaluated with Freescale Radar ICs

Isola Group, a market leader in copper-clad laminates and dielectric prepreg materials used to fabricate advanced multilayer PCBs, announced that its Astra MT laminate materials have been successfully evaluated with Freescale® Semiconductor radar ICs.

## Commercial Avionics Systems Market Driven by Modernization

The commercial Avionics Systems Market was estimated at $15,748.26 million in 2014, at a high CAGR of 7.06% from 2014–2020, to reach $23,715.24 million by 2020.

## OKI Technology Enables Mass Production of High-Frequency Boards

OKI Circuit Technology, an OKI group company responsible for printed circuit board business, has successfully developed design and mass production technologies for multi-layer printed circuit boards that support high speeds and high frequencies based on copper coin insertion.

## Military Communications Market to Hit $40B

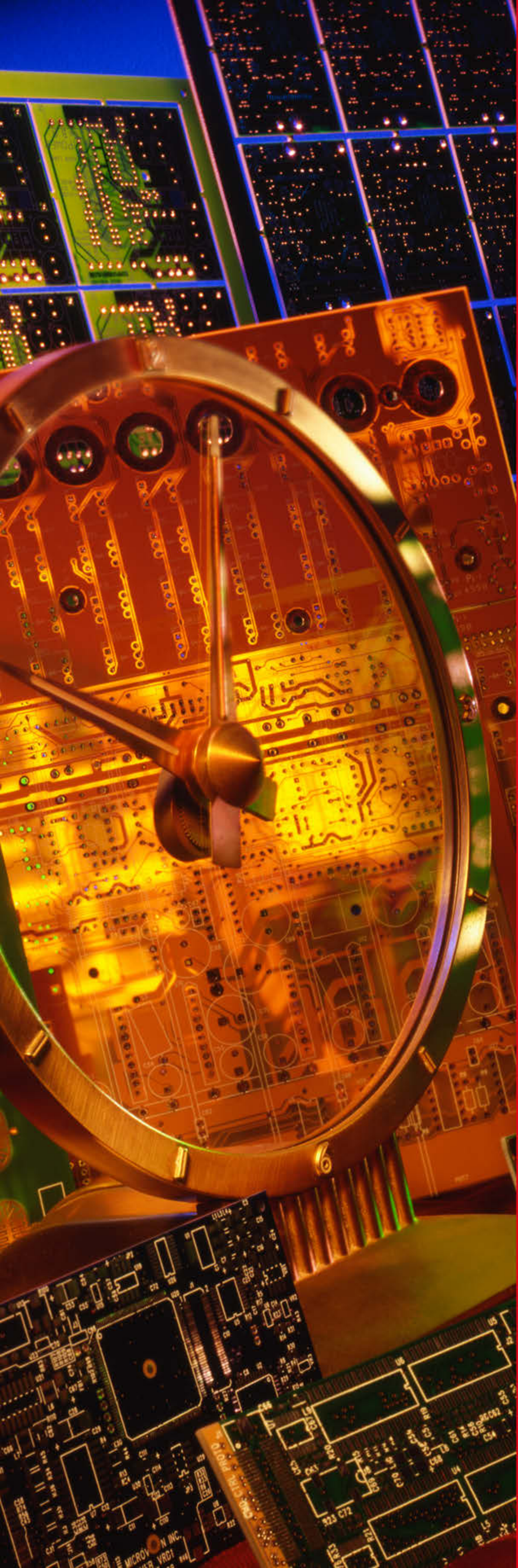
Armed forces throughout the globe rely on communication systems to enable information sharing and securely stay in constant contact. The role of these systems continues to grow in importance, with new mission areas such as the control of unmanned vehicles and time-critical targeting that is heavily reliant on network connectivity.

## NASA Unveils Latest Technology Roadmaps for Future Agency Needs

NASA has released the agency's 2015 technology roadmaps, laying out the promising new technologies that will help NASA achieve its aeronautics, science and human exploration missions for the next 20 years, including the agency's journey to Mars.

## Global Biometrics Market Revenue to Hit $67B by 2024

Tractica forecasts that the global biometrics market will increase from $2.0 billion in 2015 to $14.9 billion by 2024, with a compound annual growth rate (CAGR) of 25.3% and cumulative revenue for the 10-year period totaling $67.8 billion.



# Wearable Technology and Flexible Circuits

**by Dave Becker**
ALL FLEX

In 2012, Google introduced Google Glass, which essentially extended the functionality of a hand-held smart phone to a pair of eye glasses. It was the next step in seamlessly integrating information technology with our personal lives. With Google Glass, one can walk down a street with total awareness of the environment while viewing emails, getting weather reports or searching for the nearest restaurant. The invention of Google Glass was the kickoff to perhaps the next explosion in products called wearable technology.

Wearable technology is not exactly new; sophisticated hearing aids, bio-feedback devices, insulin pumps, blue tooth technology, and other wearable products have been around for decades. What is different today is that the electronics are smaller, faster, smarter, lighter and less expensive, all of which allows easy expansion to more applications.

Wearable technology may be the logical extension of the advancements in mobile technology, which is currently taking the form of glasses, watches, rings, wristbands and ear inserts. It is starting to move into clothing such as gloves, socks and even shirts.

Ideally, wearable technology enables us to use sophisticated information devices in a "hands free" mode, allowing us to operate more efficiently and safely. But it is much more than just "hands free"; it also enables more efficient monitoring and tracking. Applications for this technology now include law enforcement, medical, bio-technology, consumer, home automation, health and fitness, and military. New products and applications for wearable technol-

ogy are being announced almost daily.

While Google Glass was first introduced as a consumer product, the product is starting to gain acceptance in business and professional applications. Someone on the manufacturing floor can be working at a machine while viewing the latest specifications or work instructions. A doctor can be consulting with her patient while viewing medical records.

An extension of wearable is implantable or embedded technology. There has already been a great deal of discussion on implantable microchips that can carry the entire health history and identity of the user-wearer. This is essentially technology that becomes part of the human body. Embedded chips have been used with animals in studying migration patterns. In this case, the limitations may be less technology and cost and more an issue of privacy and intrusion.

Flexible circuits are an ideal fit for wearable technology. Wearable electronics need to be light, dense and bendable. While what is currently considered standard flexible circuit technology is more than adequate for many the wearable products, there are requirements that may be pushing the boundaries a bit. As electronics get integrated into clothing, the need for stretchable circuitry comes into play.

In the last decade, mobile technology has changed the social-cultural landscape, impacting billions of people around the world. Everywhere you go you will see people using their smart phone; texting, engaging in social media, shopping, searching or even making phone calls. Many experts are now predicting that wearable technology will have as great an impact on society as mobile phones. **PCB**

Dave Becker is vice president of sales and marketing at All Flex Flexible Circuits and Heaters. His column, All About Flex, will be appearing regularly in the Flex007 weekly newsletter. Contact him here.

## VIDEO INTERVIEW

### Automation in Probe Testing Provides Throughput Benefits

***by Real Time with... IPC APEX EXPO 2015***

The general migration from grid to prober for bare board testing continues, and even high-volume users now see the benefits of automation. Klaus Koziol, from atg Luther & Maelzer, explains how package testing is driving prober development.



CLICK TO VIEW

***realtimewith.com***

# Best Practices 101, Part 8: Poka-Yoke

**by Steve Williams**
STEVE WILLIAMS CONSULTING LLC

*One day, Shigeo Shingo was explaining baka-yoke, or foolproofing devices, created and implemented by workers on the Arakawa Body Company factory floor. A young woman started to cry. "Why are you crying?" Shingo asked. "Because I am not a fool," she answered. "I am truly sorry." Shigeo responded, and at that exact moment he changed the name from baka-yoke to poka-yoke: mistake-proofing devices.*
— from The Kaizen/Kaikuku Life

## Poka-Yoke

Literally translated as mistake-proofing, poka-yoke is commonly pronounced a number of ways, but the Japanese pronounce it poh-kah yo-kay. So what is poka-yoke? It is a method that uses fixtures, tooling, sensors or other devices to eliminate, or design out, the errors within a process.

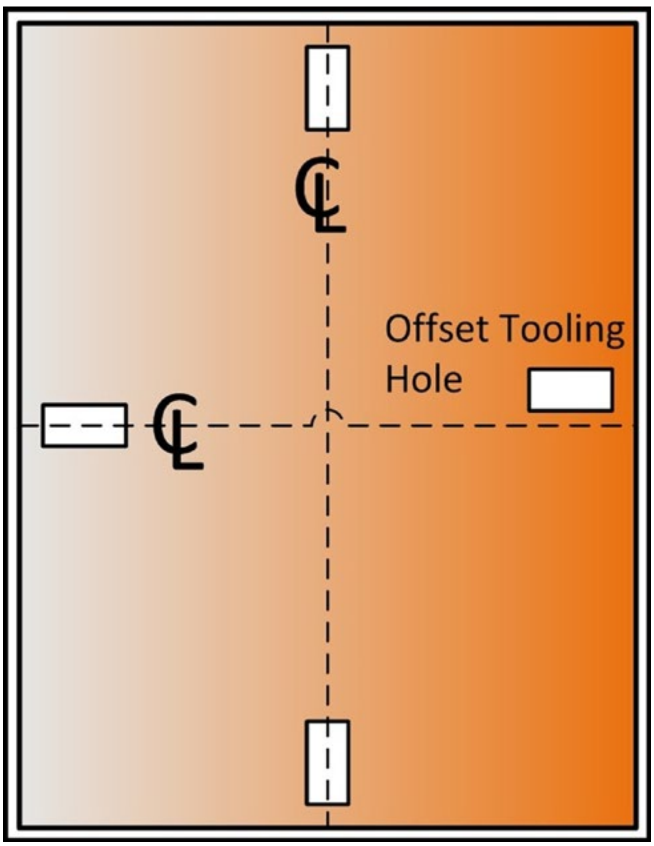



Figure 1: PCB offset tooling poka-yoke.

## Cost of Quality

Poka-yoke is important because of its purpose: to reduce the cost of quality, or more accurately stated, the cost of poor quality. The cost of quality is comprised of all the costs that relate to poor quality. As I have discussed before, the Four "Rs" are the major components of the cost of quality: repairs, rework, rejects, and returns. Each of these components can be reduced, if not eliminated, by implementing an effective poka-yoke solution.

## Defects and Process Variation

What causes defects? The answer is process variation, which begs the question, what causes process variation? Here are the 'big five' reasons for process variation:

1. Poor procedures
2. Equipment
3. Non-conforming material
4. Tooling, fixtures, jigs, etc.
5. Human mistakes

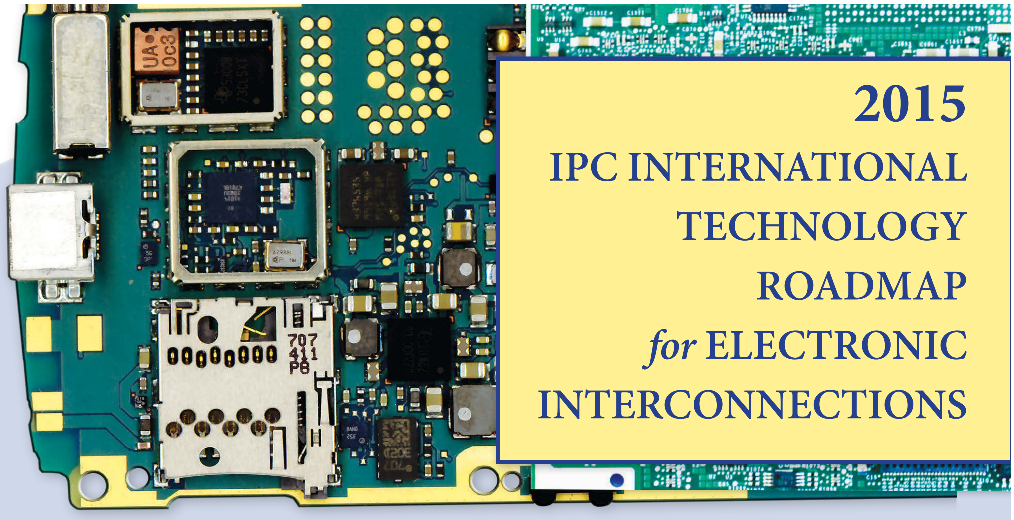
Except for human mistakes, these conditions can be predicted and addressed with corrective action to eliminate the cause of defects.

Poka-yoke detects process variation and shuts down the process before it produces an error. Poka-yoke will catch the errors before a defective part is manufactured 100% of the time. Poka-yoke focuses on the process, not on after-the-fact finger pointing.

## Types of Poka-Yoke Systems

There are two basic systems for poka-yoking a process: the control system and the warning system.

Control System: This takes the human element totally out of the equation. This is



# 2015 IPC INTERNATIONAL TECHNOLOGY ROADMAP *for* ELECTRONIC INTERCONNECTIONS

## Can You Compete in the Electronics Industry?

The *IPC International Technology Roadmap* provides valuable marketing and forecasting information and the technological requirements now and for about five years into the future to design, build, and assemble electronic interconnect products, with a heavy, historically based emphasis on printed boards and printed board assemblies that answer questions like:

- What materials will be needed in the coming years?
- What kind of equipment will need to be purchased?
- What type of training protocols will need to be adapted?

Gain valuable insights into the technology needs of tomorrow and put the informational resources of the *IPC International Technology Roadmap* to work for your long-range and strategic planning activities.

## What's New and Valuable in 2015 and Beyond

- **Laser-aided manufacturing — for yield improvements**
- **Equipment development**
- **Demand for improved vision systems required**

## What Do You Need to Prepare for?

Tremendous increase in clock speed in low-cost/high volume applications predicted over next 5 years.

Much smaller discrete components will continue shift towards emplace embedded and away from formed embedded.

Global material concerns are increasing.

Are you capable of succeeding?

With data compiled from all over the world, this comprehensive roadmap is a must-have for any organization. Get the knowledge and research at your fingertips and start making informed business decisions for today and tomorrow. Order your copy now!

**www.ipc.org/roadmap**

as close as you can come to bullet-proofing a process. These solutions truly design out the potential for producing an error or defect. A common example that everyone can relate to is the polarized plug on electrical devices. One blade is wider than the other, which matches up with a corresponding polarized outlet. This effectively makes it impossible, short of damaging the outlet, to place the plug into the outlet incorrectly. Figure 1 shows an example specific to the printed circuit manufacturing industry: the four-slot offset tooling system which makes it impossible for an operator to place a panel onto a machine incorrectly.

As a side note, it is interesting to once again observe the generational impact that technology has had on us all. In my university classes, I often use the 5-¼ inch floppy disk as an example of a product that has been poka-yoked. With the proliferation of CD/DVD burning and jump drives, I am still surprised at the number of deer-in-the- headlight looks from traditional students (students right out of high school) when I mention a floppy disk. (By the way, the clipped upper right corner assures that the disk can only be inserted one way.)

Warning System: Sometimes an automatic shutoff is not a viable option, so warning systems are implemented. Lights, buzzers, beeps, messages, etc., can be utilized to alert the operator of a potentially undesirable condition. As you might imagine, the warning system is not as bullet-proof as the control system; it requires the operator to take some action in response to the warning. A perfect example would be your vehicle, which is loaded with bells and whistles to alert the driver when some action is needed. Remember that a good poka-yoke removes the human element. The flaw in this system is, for example, that when the oil light goes off, there is nothing forcing the driver to get the oil changed. Though not as robust as the control system, it certainly is the next best option in cases like this where shutting down the process is not feasible (you wouldn't want your vehicle to shut down every time a warning light goes off).

The following are some common error-proofing devices within these systems that can be used to poka-yoke your process. Check lists, dowel and locating pins, error & alarm detectors, limit or touch switches, detectors/readers/meters/and counters, non-symmetrical tooling/fixturing.

### When to Use

Poka-yoke can be used wherever something can go wrong (basically anywhere a human is involved). It is a a tool that can be applied to any type of process be it in manufacturing or the service industry. Numerous error types are perfect for a poka-yoke solution, including:

- Processing error: Operations or tasks missed or not performed
- Setup error: Using the wrong tooling or improper machine settings
- Missing part(s): Not all parts included in the lamination, plating or other processes
- Improper part/item: Wrong part or revision used in the process
- Operations error: Carrying out an operation incorrectly
- Measurement error: Errors in inspection, test or dimensions of a part, either internally or from a supplier

### The Three Rules of Poka-Yoke

1. Don't wait for the perfect poka-yoke. Do it now!
2. If your poka-yoke idea has better than a 50% chance to succeed…Do it!
3. Do it now…improve it later!

Following these three rules will give you an excellent chance of success as you look to poka-yoke your process. **PCB**

Steve Williams is the president of Steve Williams Consulting LLC and the former strategic sourcing manager for Plexus Corp. He is the author of the books, Quality 101 Handbook and Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean. To read past columns, or to contact Williams, click here.

# 2015 Programs

## June 9

**ITI & IPC Conference on Emerging & Critical Environmental Product Requirements**

*Fort Lee, NJ, USA*

## June 9–10

**IPC Technical Education**

*Chicago, IL, USA*

Professional development courses for engineering staff and managers:

- DFX-Design For Excellence (DFM, DFA, DFR and more)
- Best Practices in Assembly
- Advanced PCB Troubleshooting
- SMT Problem Solving

## June 10

**ITI & IPC Conference on Emerging & Critical Environmental Product Requirements**

*Des Plaines, IL, USA*

## June 12

**ITI & IPC Conference on Emerging & Critical Environmental Product Requirements**

*Milpitas, CA, USA (San Jose area)*

## September 27–October 1

**IPC Fall Standards Development Committee Meetings**

*Rosemont, IL, USA*

Co-located with SMTA International

## September 28

**IPC EMS Management Meeting**

*Rosemont, IL, USA*

## October 13

**IPC Conference on Government Regulation**

*Essen, Germany*

Discussion with international experts on regulatory issues

## October 13–15

**IPC Europe Forum: Innovation for Reliability**

*Essen, Germany*

Practical applications for meeting reliability challenges like tin whiskers, with special focus on military-aerospace and automotive sectors

## October 26–27

**IPC Technical Education**

*Minneapolis, MN, USA*

Professional development courses for engineering staff and managers:

- DFX-Design For Excellence (DFM, DFA, DFR and more)
- Best Practices in Assembly
- Advanced PCB Troubleshooting
- SMT Problem Solving

## October 28–29

**IPC Flexible Circuits-HDI Conference**

*Minneapolis, MN, USA*

Presentations will address Flex and HDI challenges in methodology, materials, and technology.

## November 2–6

**IPC EMS Program Management Training and Certification**

*Chicago, IL, USA*

## November 4

**PCB Carolina 2015**

*Raleigh, NC, USA*

## December 2–3

**IPC Technical Education**

*Raleigh, NC, USA*

Professional development courses for engineering staff and managers:

- DFX-Design For Excellence (DFM, DFA, DFR and more)
- Best Practices in Assembly
- Advanced PCB Troubleshooting
- SMT Problem Solving

## December 2–4

**International Printed Circuit and APEX South China Fair (HKPCA & IPC Show)**

*Shenzhen, China*

**Questions? Contact IPC registration staff at registration@ipc.org or +1 847-597-2861**


# Recent Highlights from PCB007

## 1 A Conversation (and Day) with Joe Fjelstad

I-Connect007 Publisher Barry Matties and industry veteran Joe Fjelstad, CEO and founder of Verdant Electronics, recently spent a day together enjoying the Oregon community of McMinnville (home of the Spruce Goose), where their conversation ebbed and flowed between a wide variety of topics. The result is this five-part interview series that covers a lot of ground, from the war on process failure and the future of the electronics industry, to political shenanigans, the direction of lead-free, and more.

## 2 Design Considerations: Flexible Circuit vs. Traditional PCB

The tactics for flexible circuit design don't differ much from that of traditional PCBs. All of the typical specifications still apply and we add a few more things that require special attention. Cover layers require bigger openings than traditional solder mask, trace directions matter in the flex areas and miters should be round instead of angular.

## 3 Impact 2015: An In-Depth Look

IPC understands that presenting a unified voice for the electronics industry is essential for advancing policies that affect the industry's long-term future and strengthens the U.S. and global economy. That is why 22 IPC member-company executives descended on the nation's capital for IMPACT 2015: IPC on Capitol Hill, IPC's annual advocacy event.

## 4 AT&S Boosts Investments in Chongqing China Plant

AT&S is one of the globally leading manufacturers of high-end HDI and any-layer printed circuit boards. Key trends in this industry include the ongoing miniaturisation and increasing modularisation.

## 5 German PCB Sales Up 2.6% in March

March PCB sales in Germany went up by 2.6% compared to the same period last year, mainly driven by the industrial electronics sector, according to ZVEI PCB and Electronic Systems.

## 6 U.S. Circuit Celebrates 30 Years of PCB Fabrication

President Mike Fariba has built U.S. Circuit into a successful business through his guiding principles of hiring the best people, providing the customer with high quality products and service, and using the latest leading edge technology, all with a commitment to continuous improvement.

## 7 PCB Industry to Achieve CAGR of 4% over 2015-2020

The major drivers of the PCBs market are growing demand for 3C applications (communication, computer/peripheral, and consumer electronics), advancement in PCB technologies, and increased demand of aerospace and defense products.

## 8 AT&S Hits Record Revenues in Preliminary Results 2014/15

"We saw a disproportionately high benefit from the strong growth in the area of mobile devices, especially smartphones, and from the constantly increasing share of electronics in the automotive sector throughout the year. This led to the highest revenue in the company's history to date," says Andreas Gerstenmayer, chairman of the management board of AT&S AG.

## 9 TTM Posts Q1 Results, Sees Benefits from Acquisition of Viasystems

"We are pleased to report strong operating results in the first quarter, with revenue at the high end and non-GAAP earnings above our initial guidance ranges," said Tom Edman, CEO of TTM. "Viasystems will bring TTM meaningful strength in the automotive end market and will complement our position in other end markets, enabling us to continue to broaden our product portfolio to address an increasingly diverse set of end markets."

## 10 Continental PCB Technology Receives PACE Award

Designed for transmission control units, the bare die high-density-interconnect (BD-HDI) printed circuit board substrate technology from Continental replaces traditional ceramic solutions with high-temperature resistant materials and significantly improves technical and cost performances.

# EVENTS

**For the IPC Calendar of Events, click here.**

**For the SMTA Calendar of Events, click here.**

**For the iNEMI Calendar of Events, click here.**

**For the complete PCB007 Calendar of Events, click here.**

**JPCA 2015**
June 3–5, 2015
Tokyo, Japan

**Huntsville Expo & Tech Forum**
June 4, 2015
Huntsville, Alabama, USA

**NCEDAR 2015**
June 4–5, 2015
Bangalore, India

**IPC Technical Education Courses**
June 9–10, 2015
Chicago, Illinois, USA

**SEMICON Russia**
June 17–18, 2015
Moscow, Russia

**Philadelphia Expo & Tech Forum**
June 18, 2015
King of Prussia, Pennsylvania, USA

**Symposium on Counterfeit Parts and Materials—Tabletop Exhibition**
June 23–24, 2015
Hyattsville, Maryland, USA

**Upper Midwest Expo & Tech Forum**
Jun 25, 2015
Minnetonka, Minnesota, USA

**SEMICON West**
July 14–16, 2015
San Francisco, California, USA

**Ohio Expo & Tech Forum**
July 16, 2015
Cleveland, Ohio, USA

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# Coming Soon to *The PCB Magazine:*

*July:*
**Supply Chain Management**

*August:*
**The War on Process Failure**

*September:*
**Cars: A Driving Force in the Electronics Industry**