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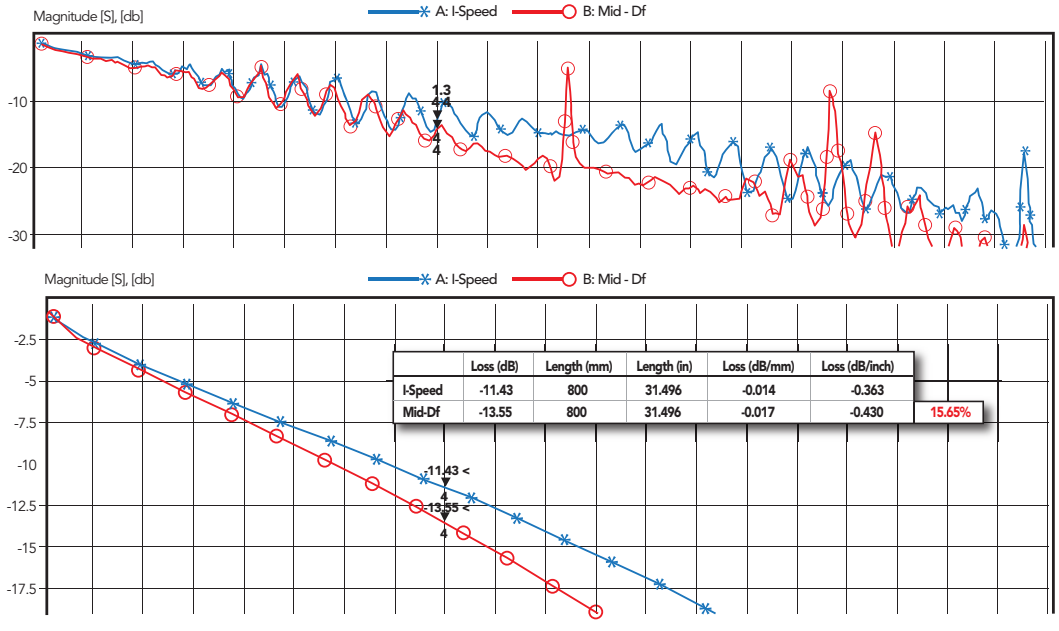

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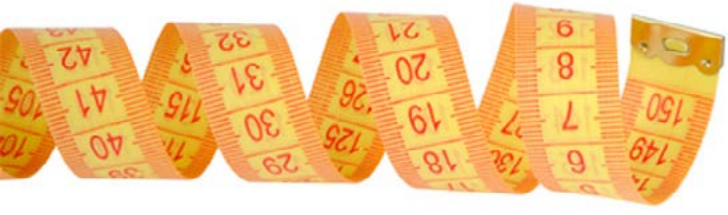
THIS ISSUE: SIMULATION & ANALYSIS

FEATURED CONTENT

Do you run simulation on your PCB designs? Circuit boards have grown increasingly faster and more complex, yet simulation is still not standard procedure, even with high-technology designs. This month, our veteran contributors discuss a variety of simulation techniques that can help you save time and avoid costly re-spins.



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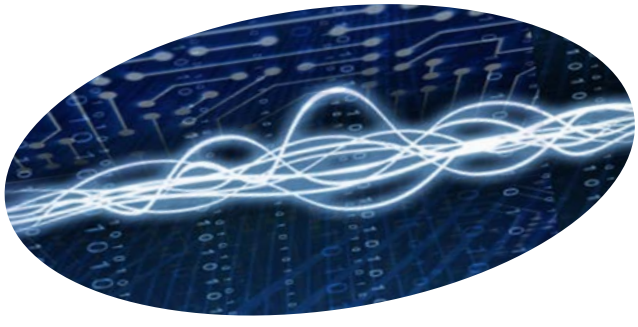

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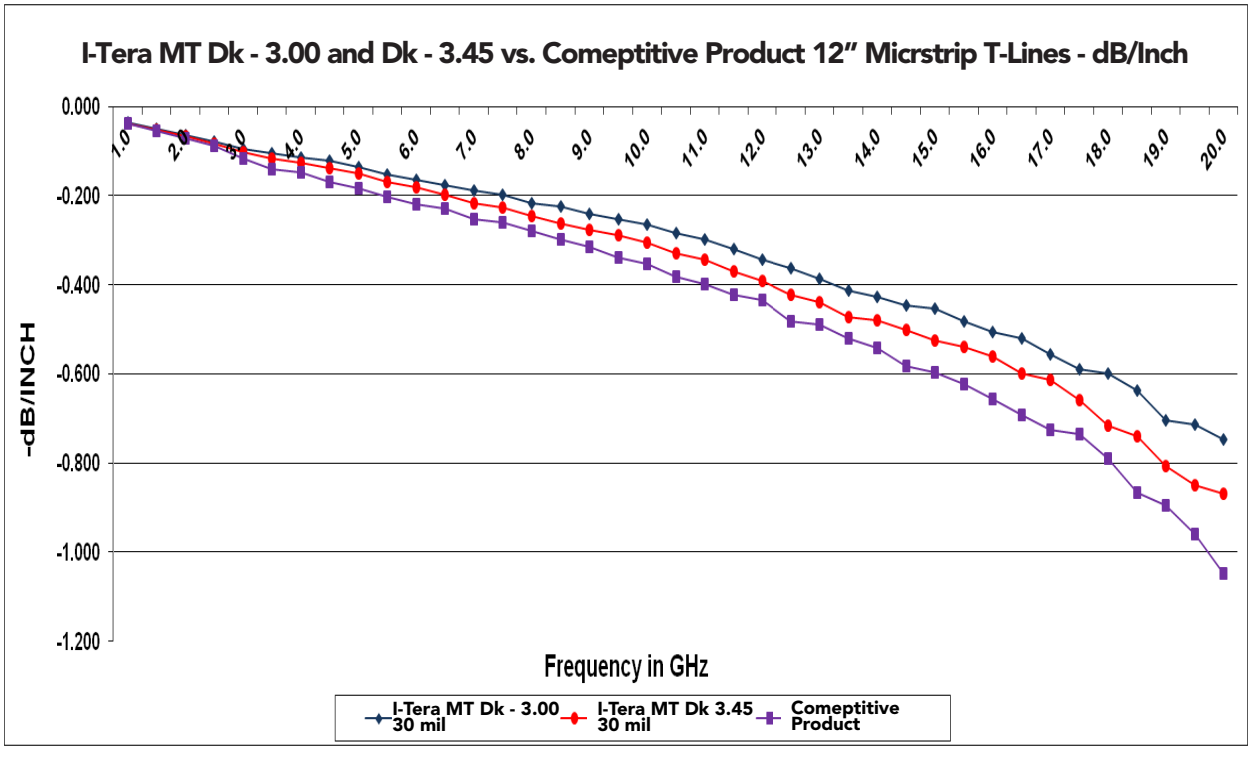

I-Tera MT shows a 15% improvement in impedance over the competitive product.

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THE SHAUGHNESSY REPORT

To Simulate or Not to Simulate?

by Andy Shaughnessy
I-CONNECT007

Years ago, very few PCB designs went through any type of simulation process. And that was just fine. Most designs were simple enough; they didn't need to be simulated.

But then high-speed design became the rule, rather than the exception. Now designers and design engineers are contending with issues such as ever-increasing edge rates, transmission line reflections, ground bounce, and crosstalk, not to mention challenges related to DDR, PCi Express, XAUI, and SERDES.

Simulation software became a big segment of our industry. Over the past few decades, we've seen companies like Ansoft, Agilent, CST, E-System Design, HyperLynx, Sigrity, Simberian, SiSoft, and Zeland develop PCB simulation and analysis solutions.

These companies used to exhibit at all of the industry trade shows, from DesignCon to MTT/S to PCB West. But over the years, many of them have been absorbed by the "big guys."

The EDA companies saw plenty of value in the smaller simulation software companies, not to mention the technical ability behind it. For a comparatively small amount of money, an EDA company could dramatically improve its simulation software lineup.

So Ansoft was acquired by ANSYS, HyperLynx and Zeland are now part of Mentor Graphics, and Sigrity was purchased by Cadence last year. Only Agilent, CST, E-System Design, Simberian and SiSoft remain independent. Agilent may be too big to be acquired, but you have to wonder whether Mentor, Cadence or Zuken have their eyes on any of the other four.

They'd all be worth acquiring just for the engineering talent alone.

Still, there seems to be a disconnect; some OEMs just don't see any reason to run simulation. I talk with plenty of designers who don't simulate their designs, and these guys aren't designing yesterday's technology. They're creating some seriously cutting-edge, multigig boards. I've seen stats showing that only about half of all PCB designs are simulated, and that seems pretty accurate to me.

Do you simulate your designs? Send me an e-mail and let me know why or why not. This is definitely a topic worth revisiting.

Happy Birthday

Before I sign off, I'd like to offer a few birthday wishes. HyperLynx, Mentor Graphics' simulation software tool, is celebrating its 25th birthday this year. The company HyperLynx

TO SIMULATE OR NOT TO SIMULATE? *continues*

was founded in 1988, aiming to bring high-speed design tools to the then-nascent PC world. The first HyperLynx tool was LineSim, followed by BoardSim and the EMC analysis tool SpectralSim. HyperLynx stayed involved in the industry, and management co-founded the IBIS Open Forum in 1993. In 1997, HyperLynx was acquired by PADS, which in 2000 was purchased by Innoveda. Mentor then acquired Innoveda in 2002. Mentor demonstrated the newest HyperLynx release at DesignCon in January.

And Intercept Technology is turning 30 this year. When Intercept started out as an engineering consulting firm in 1983, founder Steve Klare had no intention of running an EDA software company. But after a decade of dealing with the challenges related to the CAE and CAD software of the time, Intercept began developing its own EDA tools. The company recently redesigned the GUI of its Pantheon design suite, which had remained unchanged, and still loved by many users, since its introduction in 1994. Intercept now offers solutions for RF and hybrid design, as well as schematic and library management tools.

We always hear that our industry is static, that PCB designers and design engineers are afraid of change. Well, there might be some truth to that. After all, most of us are in our 40s and 50s, and it's only natural that we become set in our ways.

But the industry is constantly changing. And isn't that why we enjoy our jobs in the first place? **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.

IPC: December 2012 Shipments, Bookings Down

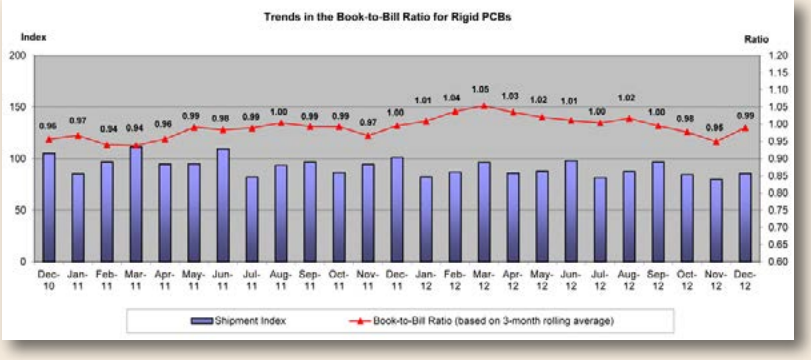
IPC has announced the December findings from its monthly North American Printed Circuit Board (PCB) Statistical Program.

Rigid PCB shipments were down 16.1% in December 2012 from December 2011, and bookings decreased 8.8% year over year. Year to date, rigid PCB shipments declined 5.5% and bookings decreased 1.7%. Compared to the previous month, rigid PCB shipments were up 7.1% and rigid bookings increased 19%. The book-to-bill ratio for the North American rigid PCB industry in December 2012 recovered to 0.99.

Flexible circuit shipments in December 2012 were up 6.7%, and bookings were up 9.4% compared to December 2011. Year to date, flexible circuit shipments decreased 1.5% and bookings decreased 10%. Compared to the previous month, flexible circuit shipments decreased 7.4%, but flex bookings were up 20.2%. The North American flexible circuit book-to-bill ratio improved to 0.84.

For rigid PCBs and flexible circuits combined, industry shipments in December 2012 were down 14.5% and bookings decreased 7.5%, compared to December 2011. Year to date, combined industry shipments were down 5.2% and bookings were down 2.4%. Compared to the previous month, combined industry shipments for December 2012 increased 5.7% and bookings increased 19.1%. The combined (rigid and flex) industry book-to-bill ratio in December 2012 rose to 0.98.

"North American PCB book-to-bill ratios appear to have begun recovering after a downward trend that began in the second quarter of 2012," according to Sharon Starr, IPC director of market research. "The industry's sales ended 2012 at 5.2% below 2011."



Measuring Correlation to 50 GHz and Beyond

by Yuriy Shlepnev
SIMBERIAN INC.

SUMMARY: Four essential elements of electromagnetic signal integrity analysis guarantee successful design of PCB and packaging interconnects up to 50 GHz and beyond: bandwidth and quality of S-parameter models, broadband material characterization and identification, localization of all elements of a channel and systematic benchmarking process. All of these elements of the design flow lead to success, and neglecting or missing even one of them may compromise the whole project.

Introduction

Faster data rates drive the need for accurate models for data channels, specifically for PCB and packaging interconnects. Now, 10 gigabit Ethernet is practically in the mainstream, and 25 gigabit is coming out. The spectrum of signals in these channels ranges from DC or MHz frequencies up to 20-50 GHz and beyond (into centimeter and millimeter wavelengths) and imposes very special requirements on the interconnect modeling and design. Using simplified models or none at all may result in complete failure of such channels and require multiple iterations to fix, and this may be not possible. What is the best way to model such high-speed interconnects? It obviously depends on a problem to solve. For signal integrity analysis, interconnects can be formally divided into transmission line segments (planar or cables) and discontinuities or transitions in lines such as vias and connectors as schematically shown in Figure 1.

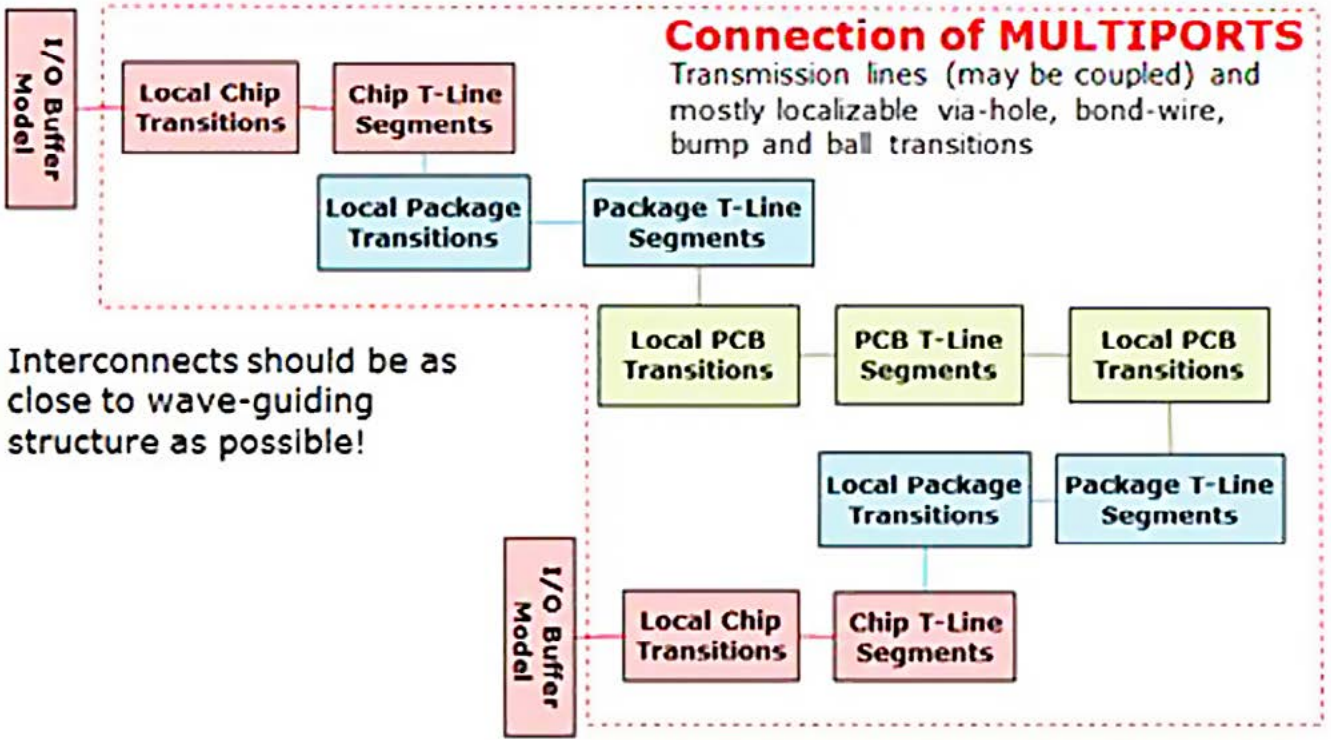


Figure 1: Interconnect model as connection of multiports. In general, the goal of interconnect design is to make it as close to a localized wave-guiding structure as possible and thus predictable with the analysis.

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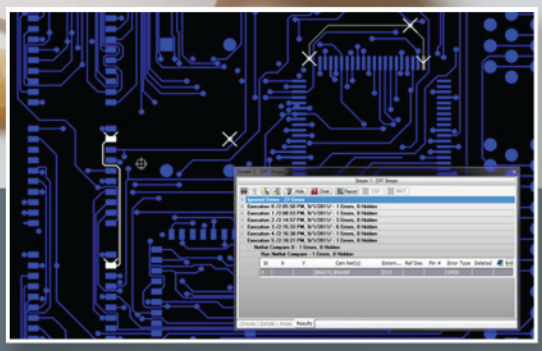
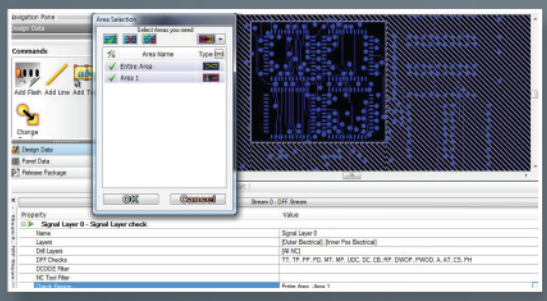


Netlist errors are quickly validated in DFMStream



Define DFM checks by area so components such as BGAs can be verified with unique rules different from rest of design

DownStream Technologies

Multiport models of components are built separately with static or electromagnetic analysis, measurements or obtained from component vendors and then united into a complete channel model. This technique was developed from microwave application and is known as decompositional electromagnetic analysis (also known as "divide and conquer" or the segmentation technique). It is also widely used in signal integrity analysis tools for digital applications. Still, the limitations of this technique and key elements that lead to success in the case of digital interconnects is a subject of ongoing research (see the latest DesignCon papers, for instance). Interconnects typically require analysis over a much larger frequency band, and may contain components that have not being used in microwave applications. This article will explain four essential elements of the decompositional electromagnetic signal integrity analysis that guarantee measurement correlation up to 50 GHz and beyond:

1) Quality of S-parameter models of interconnects (bandwidth, sampling, passivity and causality).
2) Broadband dielectric and conductor roughness models (important for analysis of transmission lines).
3) Localization property and de-embedding of discontinuities (possibility to be analyzed in isolation).
4) Procedure to validate models with measurements on a set of standard test structures (benchmarking).

Quality of S-parameter Models

Any element of a linear time-invariant data channel can be modeled as a multiport described with S-parameter models[1, 2]. Multiport is a natural and scalable black-box description of linear structures smaller, comparable to, or larger than the wavelength. In decompositional analysis, multiport parameters of transmission lines, via holes and other components are united and then simulated with models of the transmitter and receiver as schematically shown in Figure 1. Multiports are often described with S-parameter models produced by circuit and electromagnetic simulators, VNAs and TDNAs. Very often such models have issues and may be not suitable for consistent broadband frequency, time-domain and compliance analyses of interconnects. Analysis to measurement correspondence is possible only with multiport models that have sufficient bandwidth and pass quality control. This is one of the key elements in the design success.

S-parameter models are usually band-limited due to the limited capabilities of solvers and measurement equipment. Model should include the DC point or allow extrapolation, and high frequencies defined by the signal spectrum. If a model does not contain the DC point, the lowest frequency in the sweep should be below the transition to skin effect (1-50 MHz for PCB applications), or below the first possible resonance in the system defined as

$$f_l < \frac{c}{4L \times \sqrt{\varepsilon_{eff}}}$$

to allow extrapolation to DC. Here L is total physical length of the system, c is speed of light and ε_{eff} is effective dielectric constant. The highest frequency in the sweep must be defined by the required resolution in time-domain or by spectrum of the signal[4]. The highest frequency can be defined either with signal rise time tr as

$$f_h > \frac{1}{2t_r}$$

or with the main harmonic fs1 as

$$f_h > K \times f_{s1}.$$

Here K may range from 2 to 5, depending on the actual attenuation in the channel. All models for a channel interconnects should satisfy the target bandwidth requirement. Otherwise they have to be discarded and rebuilt.

In addition to being band-limited, most interconnect component models come in the form of Touchstone models[3]. Touchstone models are just S-parameters defined at a set of frequencies. Interpolation or approximation of tabulated matrix elements may be necessary both for time- and frequency-domain analyses. Appropriate sampling is very important for DFT and convo-

lution-based time domain analysis algorithms[4], but not so for algorithms based on rational approximation. In general, there must be 4-5 frequency points per each resonance. In addition, the electrical length of a system should not change more than one quarter of wavelength between two consecutive frequency points

$$df < \frac{c}{4L \times \sqrt{e_{eff}}}$$

Under-sampling typically occurs at lower frequencies and may lead to defects both in frequency and time-domain analyses. Such models have to be discarded and rebuilt.

On top of being band-limited and the risk of possible undersampling, these models can be distorted with the measurement or simulation artifacts that are not so easy to detect. For instance, model convergence issues, fast frequency sweeps, non-conservative ports, and unaccounted high-order modes in electromagnetic analysis may cause model distortions. Measurement noise, calibration and measurement equipment problems can also lead to defective models. In general, those are human mistakes of tools developers and users.

How best to estimate the quality of S-parameter models to make sure that the models are suitable for analysis? S-parameters quality metrics have been recently introduced[5, 6] to simplify the task. Metrics for passivity, reciprocity and causality computed for band-limited discrete models can be used for preliminary analysis of the quality of S-parameters. The metrics range from 0 to 100; zero means bad and 100 is good. Ranges for acceptable and questionable models are defined on the base of analysis of thousands of models. An example of preliminary analysis of a set of models in Simbeor Touchstone Analyzer tool[7] designed for automation of S-parameter quality assurance is shown in Figure 2.

Note that preliminary quality estimation is done for a discrete and band-limited data set and, thus, is incomplete. Though, it allows detecting unacceptable violation of passivity and reciprocity. If passivity or reciprocity metrics are close to zero, the model must be discarded and

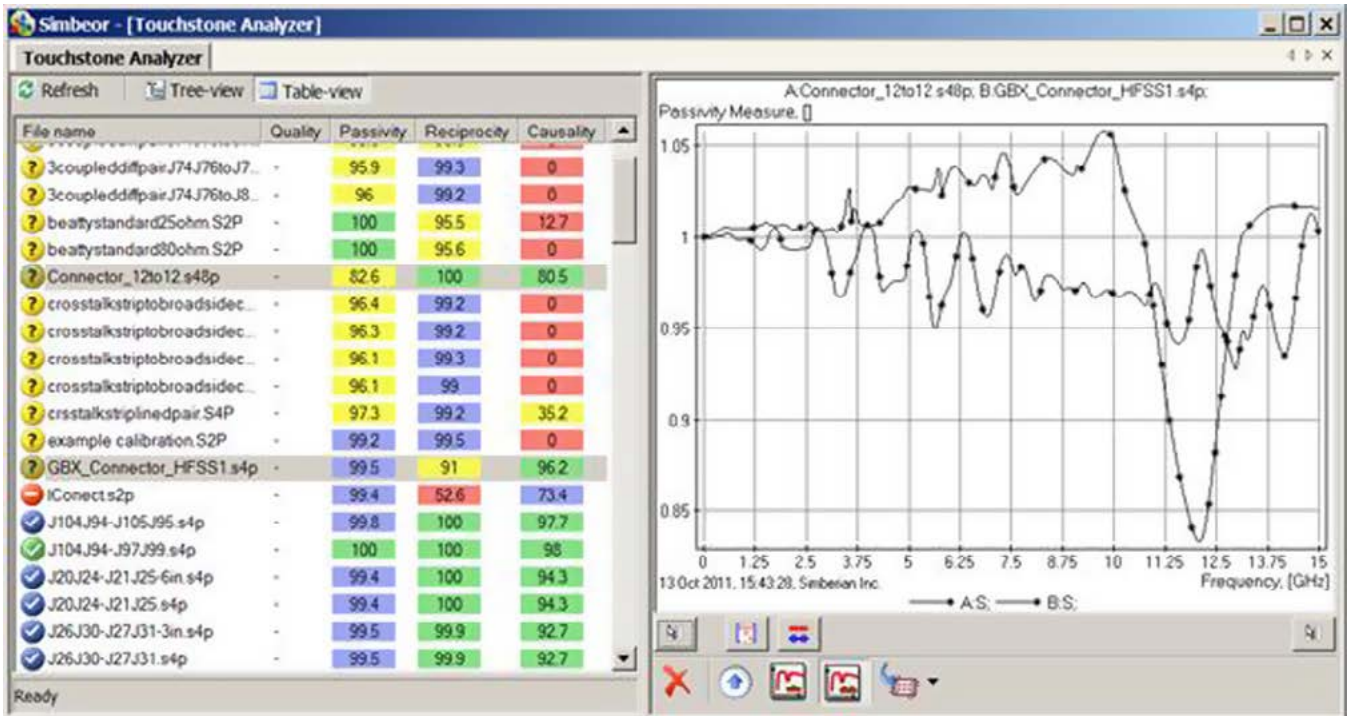


Figure 2: Example of preliminary analysis of Touchstone models quality in Simbeor Touchstone Analyzer. Good metrics are shown in green; acceptable in blue; questionable in yellow; and bad is red. Graph on the right is adjusted for passivity measure for two selected models – passivity violated if the measure is above unit.

MEASURING CORRELATION TO 50 GHZ AND BEYOND *continues*

rebuilt. Large violations of preliminary causality metric in computed models point at undersampled data – such models have to be also rebuilt. Large causality violation in measured data may occur because of measurement noise and can be fixed with the rational approximation. A model ranked as good with preliminary metrics may still have hidden defects and may not allow accurate interpolation or extrapolation for purpose of time-domain analysis for instance. Rigorous estimation of passivity and causality can be done only for a frequency-continuous model defined from DC to infinity. Such models can be built with the rational approximation of the original tabulate data.

Rational macro-models are frequency-continuous models defined from DC to infinite frequency and can be used for the final quality estimation. High-quality tabulated models can be accurately approximated with passive rational macro-models. The final quality metric with a range from 0 to 100 can be constructed using the root-mean square error (RMSE) of the passive rational approximation as[6]

$$Q = 100 \cdot \max\left(1 - RMSE, 0\right)\%$$

S-parameters approximated with rational functions are causal by definition in case passivity is ensured from DC to infinite frequencies. An example of the final model quality estimation with rational macro-models is shown in Figure 3. Low-quality metrics mean that the tabulated model cannot be accurately interpolated and extrapolated with a causal passive model and must be discarded. After model quality is ensured, it can be further exported and used as a broadband SPICE macro-model (BB SPICE) or improved by resampling. Note that BB SPICE models are frequency-continuous and contain extrapolation to DC and infinity and, thus, guarantee consistent analyses both in frequency and time-domain in practically all tools.

Broadband Dielectric and Conductor Roughness Models

The largest part of interconnects can be formally defined and simulated as transmission

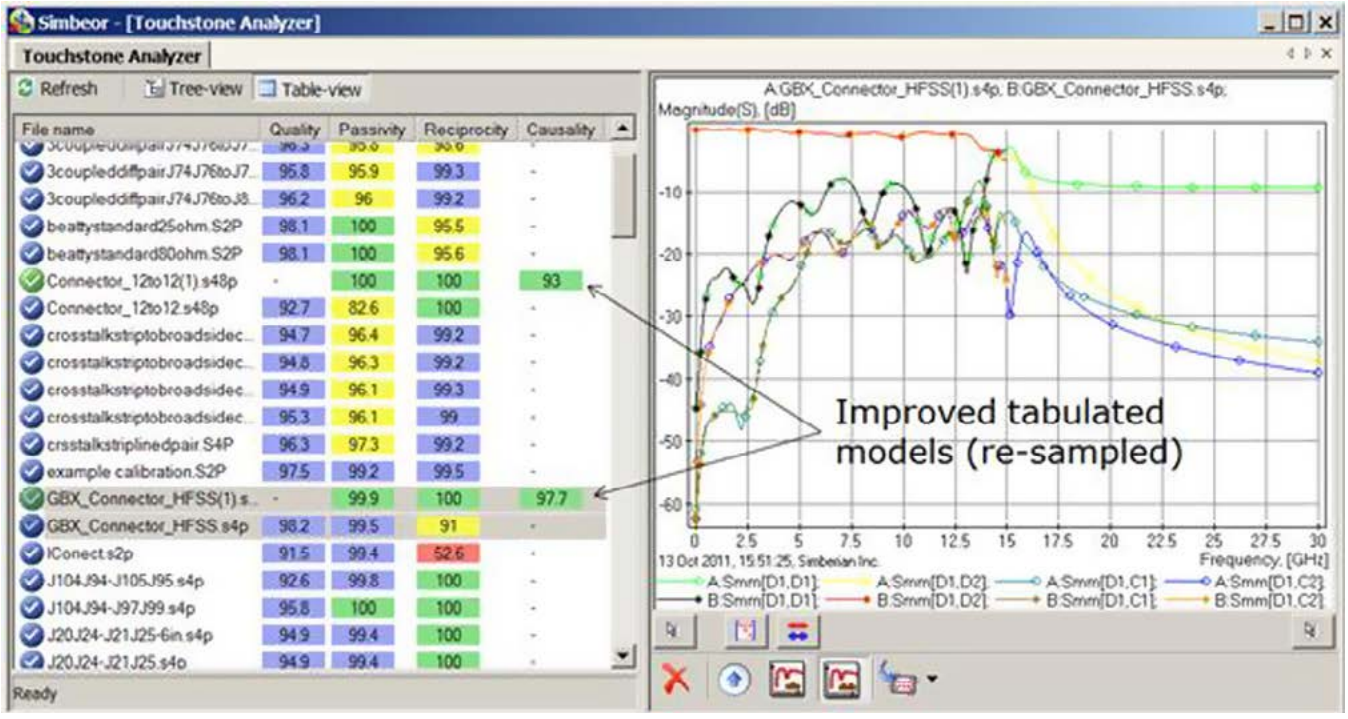


Figure 3: Example of the final model quality analysis in Simbeor Touchstone Analyzer. Model icons and the "Quality" column illustrate the model quality estimated with the passive rational approximation (good = green, blue = acceptable). Columns passivity and reciprocity show quality of the original tabulated data. Graph on the right is adjusted to compare magnitudes of the original and "improved" models.

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line segments. Models for transmission lines are usually constructed with static or electromagnetic field solvers. Transmission lines with homogeneous dielectrics (striplines) can be effectively analyzed with quasi-static field solvers, and lines with inhomogeneous dielectric may require analysis with a full-wave solver to account for the high-frequency dispersion[8, 9]. Accuracy of transmission line models is mostly defined by availability of broadband dielectric and conductor roughness models. Wideband and multipole Debye models[9] are examples of widely used dielectric models suitable for accurate analysis of PCB and packaging interconnects. Parameters for such models are usually not available from manufacturers and have to be identified.

To simulate the effect of conductor roughness, modified Hammerstadt[10] and Huray's snowball conductor roughness models[11] can be used effectively, but parameters for such models are not readily available from manufacturers. Makers of dielectrics provide dielectric parameters at 1-3 points in the best cases; those points may be acceptable to define a wideband Debye model. Copper laminate manufacturers typically do not offer parameters for electrical roughness models. Thus, meaningful interconnect design and compliance analysis must start with the identification or validation of dielectric and conductor roughness models over the frequency band of interest. Even electromagnetic analysis of interconnects without such models may simply be inaccurate and useless.

Accurate material characterization up to a target frequency is the most important element for design success. The simplest procedure for such validation or identification is based on generalized modal S-parameters (GMS-parameters)[12]. S-parameters are measured for two line segments with substantially identical transitions and cross-sections, converted into reflectionless GMS-parameters, and material models are then identified by matching computed and measured GMS-parameters. The procedure is automated in Simbeor software. As an example of material parameters identification up to 50 GHz (for 25-30 Gbps data channel), we use measured data provided by Molex engineer David Dunham for one of the material characterization boards made of Nelco N4000-13EP dielectric and VLP copper[13]. A set of 2-, 4- and

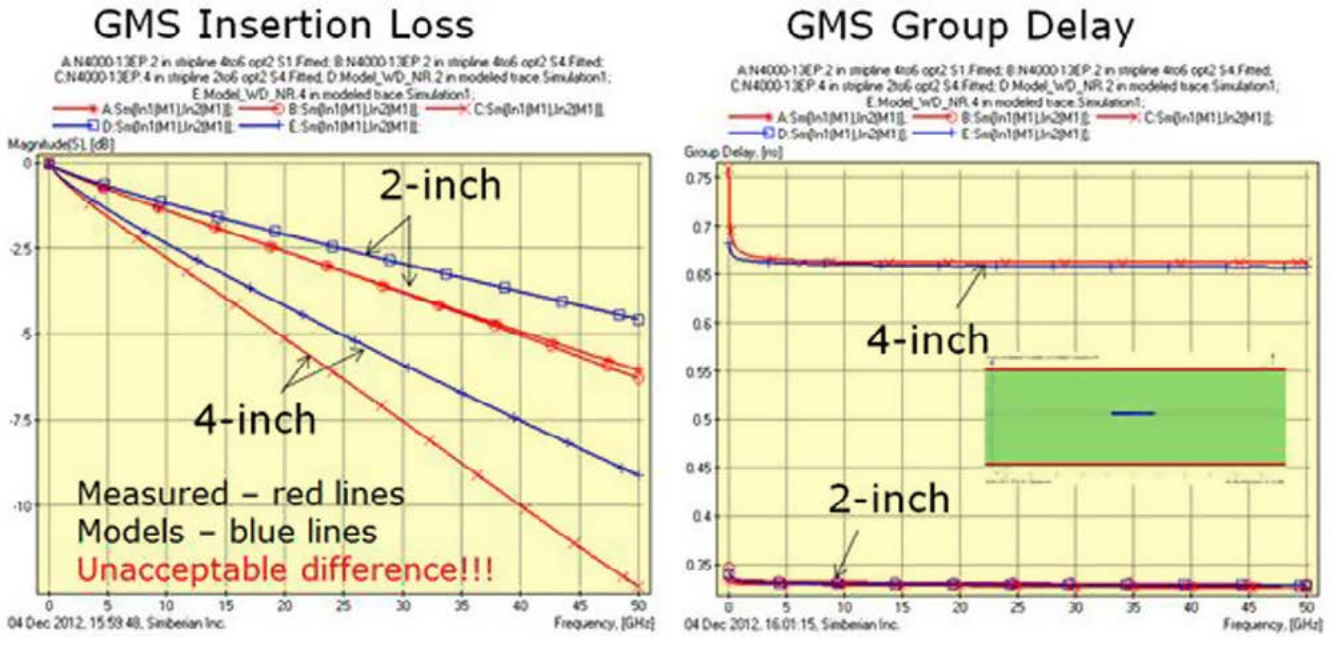

Figure 4: Measured (red lines) and computed (blue lines) generalized modal insertion loss (left plot) and group delay (right plot) for 2- and 4-inch strip line segments (dielectric model from manufacturer and smooth conductor model).

6-inch stripline segments was used to extract reflectionless GMS-parameters for 2-inch and 4-inch line segments as shown in Figure 4. The dielectric specifications show that this dielectric may have dielectric constant (Dk) from 3.6 to 3.7 and loss tangent (LT) from 0.008 to 0.009.

If we compute GMS-parameters for 2- and 4-inch segments using electromagnetic analysis with a wideband Debye model and Dk=3.8 and LT=0.008 defined at 10 GHz, the difference in the measured and computed group delay is very small, but the difference in GM insertion loss is huge, as illustrated in Figure 4. Dk in the model is slightly increased to match group delays – that increase can be explained by anisotropy of the dielectric. Horizontal component of the Dk for layered glass-resin dielectrics can be up to 20% larger[14] and the manufacturer probably used wider strips to identify the dielectric. Wider strips have less energy in the horizontal component of electric field and predict smaller Dk.

What about the loss tangent – how can we explain such huge difference in the predicted and measured IL? Typically this situation is explained as wrong data provided by the manufacturer. In this case LT should be increased to 0.0112 to have an acceptable match for insertion loss. Another option is to assume that the dielectric data from the manufacturer are actually correct, and attribute all observed excessive losses to the conductor roughness. As shown in Figure 5, nearly perfect correspondence of measured and computed models can be achieved with the modified Hammerstadt model with a roughness parameter of 0.27, roughness factor of 4 and conductor resistivity adjusted to 1.1 (relative to resistivity of annealed copper).

As the result of this simple example we ended up with two models – with LT=0.0112 and no roughness and with LT=0.008 (as in the specs) and additional model for conductor roughness. Which one is correct? Both models are suitable for the analysis of the 8.5 mil stripline on this board. However, if strips with different width are used, the model without the roughness model will be much less accurate. For instance, the model without roughness predicts up 40% smaller losses for differential strip with 4 mil wide strips and 4 mil spaces. The model with the rough conductor is expected to produce more accurate insertion loss estimation for a broad range of strip widths. This example illustrates a typical situation and the im-

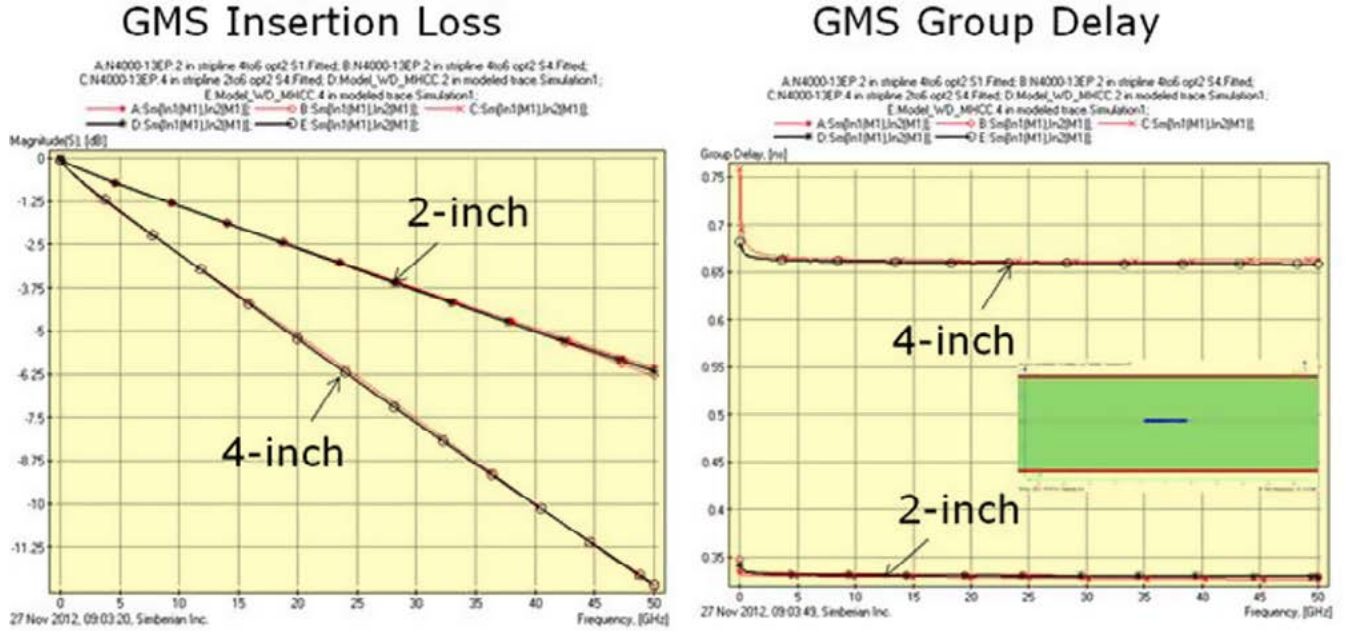

Figure 5: Measured (red lines) and computed (black lines) generalized modal insertion loss (left plot) and group delay (right plot) for 2- and 4-inch strip line segments (dielectric model from manufacturer and rough conductor model with SR=0.27, SR=4).

portance of dielectric and conductor roughness model identification to measure correspondence for a set of transmission lines on a particular board for a target frequency range.

Localization Property and De-Embedding Discontinuities

Ideally, all interconnects should look like uniform transmission lines with specified characteristic impedance. In reality, a channel is typically composed of transmission lines of different types (microstrip, stripline, coplanar, coaxial, etc.) and transitions between them such as vias, connectors, breakouts and so on. Even if we maintain the same impedance for lines of different types, the transitions may be still reflective due to physical differences in cross-sections of the connected lines (coaxial and micro-strip for instance). The reflections cause additional losses and resonances and, thus, unwanted signal degradation. The effect of the transitions can be accounted for with models built with a full-wave 3D analysis. If such analysis is possible in isolation from the rest of the board up to a target frequency, the structure is called localizable[15]. Structures whose behavior is dependent on board geometry are called not localizable, and they should not be used for multi-gigabit interconnects in general. Analysis of such structures is possible only at the post-layout stage with substantial simplifications that degrade accuracy of the model at frequencies above 3-5 GHz. In other words, only localizable transitions and discontinuities must be used to design predictable interconnects at frequencies above 3-5 GHz – this is one of the most important elements of successful design.

How best to estimate the localization property of a transition? The simplest way is to run electromagnetic analysis of the structure with different boundary conditions or simply change simulation area size and evaluate the differenc-

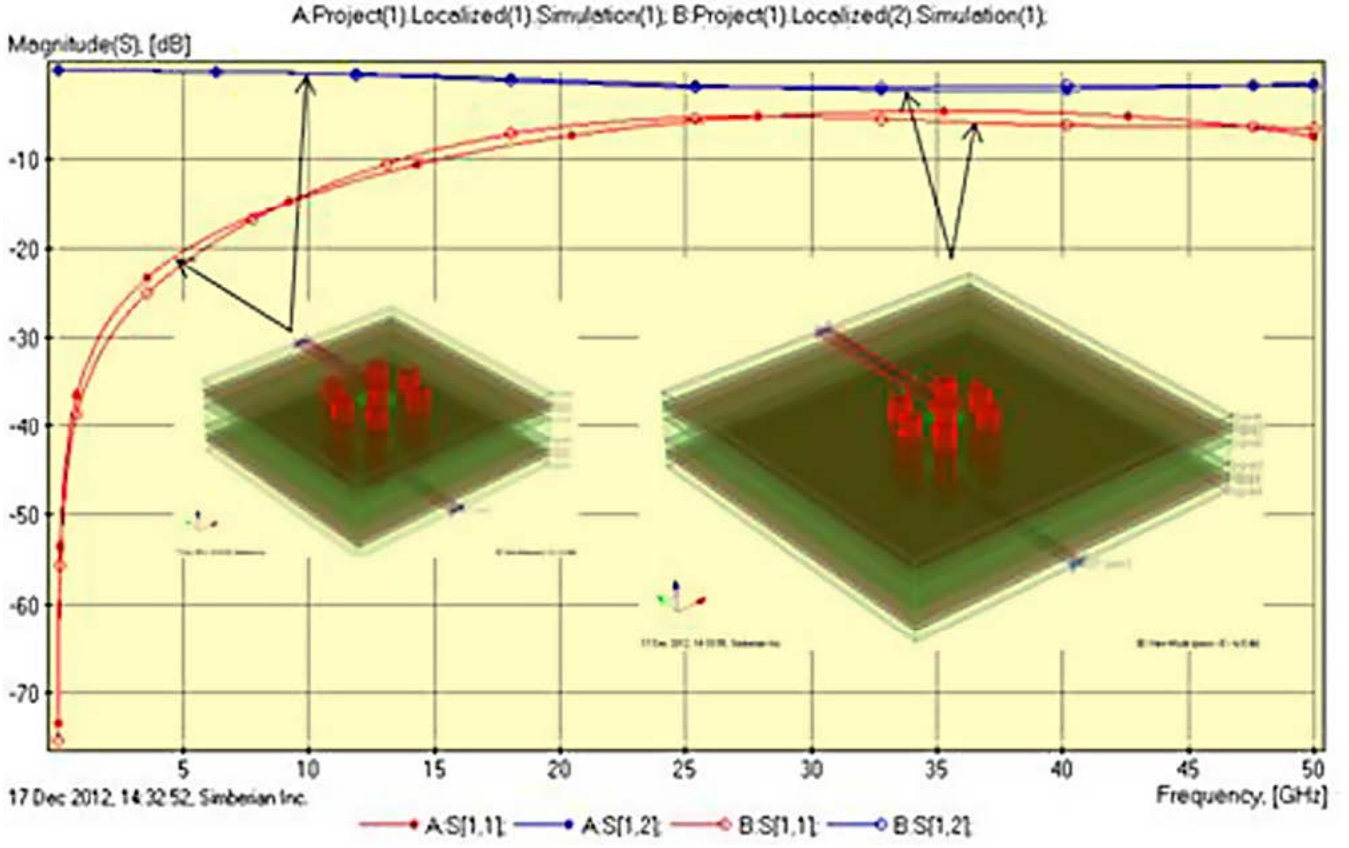

Figure 6: A localization property evaluation for a single via with six close stitching vias. Increase of simulation area size just slightly changed computed reflection (red lines) and insertion loss (blue lines).

es. An example of the localization evaluation for a single via with six stitching vias is shown in Figure 6. The structure can be considered as localizable up to 50 GHz. The via in this example is localizable, but not optimal – the reflection loss may be not acceptable if multiple vias are used in a channel. Further via optimization can be performed in Simbeor Via Analyzer and SiTune optimization tools.

In this comparison of S-parameters of two vias simulated in different area, de-embedded transmission line ports are used to reduce the numerical reflection and to shift the phase reference plane closer to vias and to have S-parameters describing exactly the same portion of the geometry. The quality of such numerical de-embedding defines the quality of the final interconnect model. The simplest way to evaluate the de-embedding quality is to simulate a 90-degree segment of ideal 50-ohm stripline as suggested here[16]. This simple test allows rigorous estimation of de-embedding accuracy and dynamic range. Another way is to simulate a T-line segment and concatenate the models into a longer segment – there should not be reflections observed at the connection points. If substantial reflections observed in such numerical experiment, the models are not suitable for the decompositional analysis.

Analysis to Measure Validation – Benchmarking

Finally, how to make sure that the interconnect analysis works up to the target frequency and what is the problem if it does not? The best way to evaluate the accuracy of analysis is to build a validation or benchmarking board and compare analysis results with measurements. Benchmarking is one of the most important elements of the design success. First of all, such board should include a set of structures to identify all dielectrics and conductor roughness

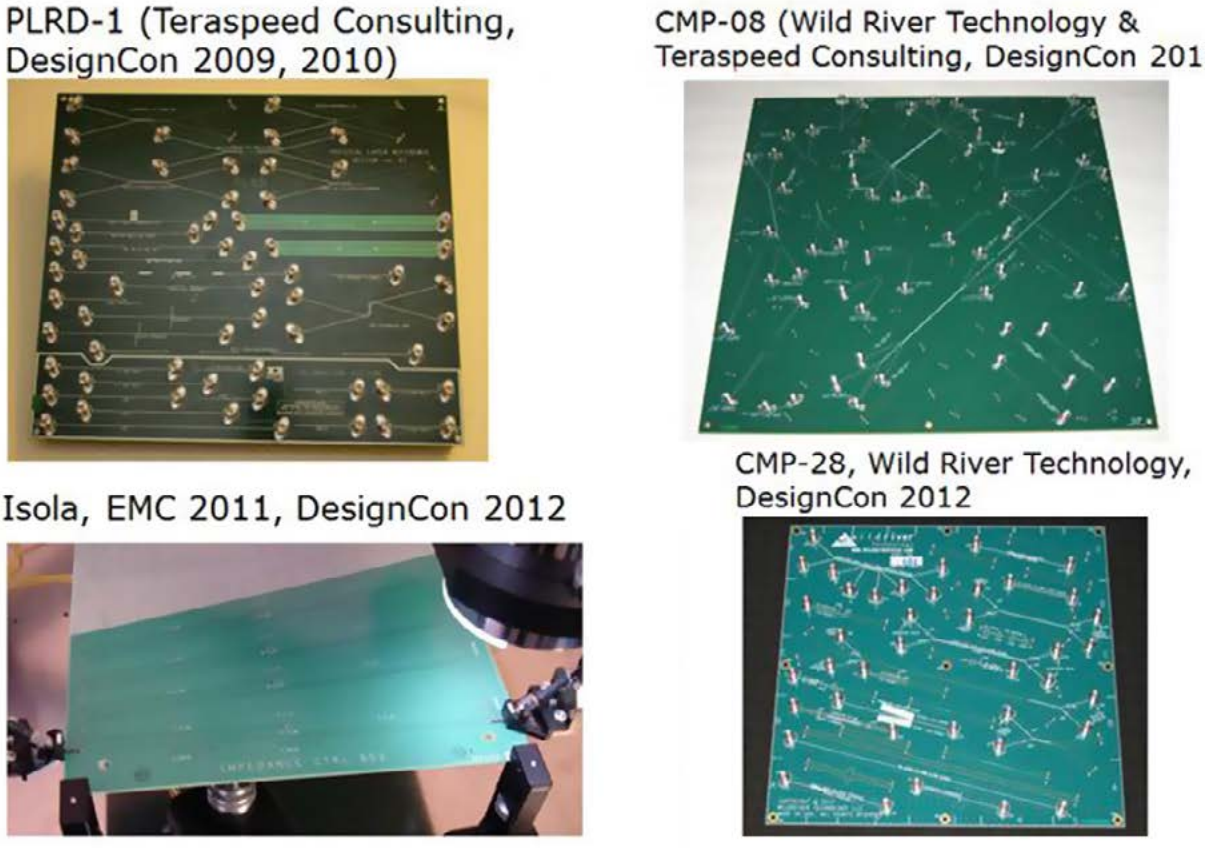

Figure 7: Examples of benchmarking boards featured in References 12 and 17 (top left), Reference 18 (top right), Reference 19 (bottom left), and Reference 20 (bottom right).

models. There must be at least one pair of lines per material model to separately identify models for solder mask, core and prepreg dielectrics or resin and glass, conductor roughness, plating material and so on. Identification of two models at the same time may lead to multiple possibilities and is problematic, as was pointed out at the dielectric and roughness model identification section. Benchmarking should also include a set of structures to identify the accuracy for transmission line models with possible coupling, resonant structures (i.e., Beatty standards or other type of planar resonators) and typical discontinuities (channels with single and differential vias, for instance). Examples of benchmarking boards[12, 17, 20] developed and investigated up to 50 GHz are shown in Figure 7.

Considering the benchmarking process, identified material models must be consistently used for the analysis of all structures on the board. Tweaking dielectric or conductor roughness models for each structure for instance should be strictly prohibited. Possible discrepancies reveal either limitations of a tool or board design or manufacturing defects that altered the expected behavior. The source of the discrepancy must be investigated. The best choice for benchmarking measurement is VNA with the target frequency bandwidth. Either coaxial connectors or probe launches can be used. Probe launches are easier to model, but the measurement have to be done with a probe station – handheld probes are simply not suitable at microwave frequency range.

In the case of connectors with launches, they can be de-embedded or simulated too (more difficult due to unknown material properties). TRL-type de-embedding can be used for PCBs[17], but additional structures may be needed for the de-embedding (they can be also used for the material parameters identification). Note that simple T-matrix de-embedding simply does not work for PCB applications due to inhomogeneity of dielectrics and large manufacturing variations. Finally, measured and computed magnitudes and phases or group delays for all S-parameters have to be compared. Just insertion loss comparison is incomplete and may be misleading. Always compare phase or group delay and also reflection parameters.

Conclusion

Four essential elements that guarantee successful design of PCB and packaging interconnects up to 50 GHz and beyond have been outlined in this article. Bandwidth and quality of S-parameter models, broadband material characterization and identification, localization of all elements of a channel and systematic benchmarking process are equally important elements of successful design. If even one element is missing or neglected, it may compromise the whole project. **PCBDESIGN**

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Yuriy Shlepnev, Ph.D., is founder and president of Simberian Inc. He previously served as principal engineer at Mentor Graphics and director of the Electromagnetic Group at Eagleware Corporation.

video interview

Simberian: High-End Simulation For Designers

by Real Time with... PCBDesign007

Yuriy Shlepnev discusses his latest release, Simbeor 2013. Simbeor did not win a Design Vision Award at DesignCon this year, but Simbeor has already taken home the award two years in a row. Shlepnev also shows off one of his latest projects.

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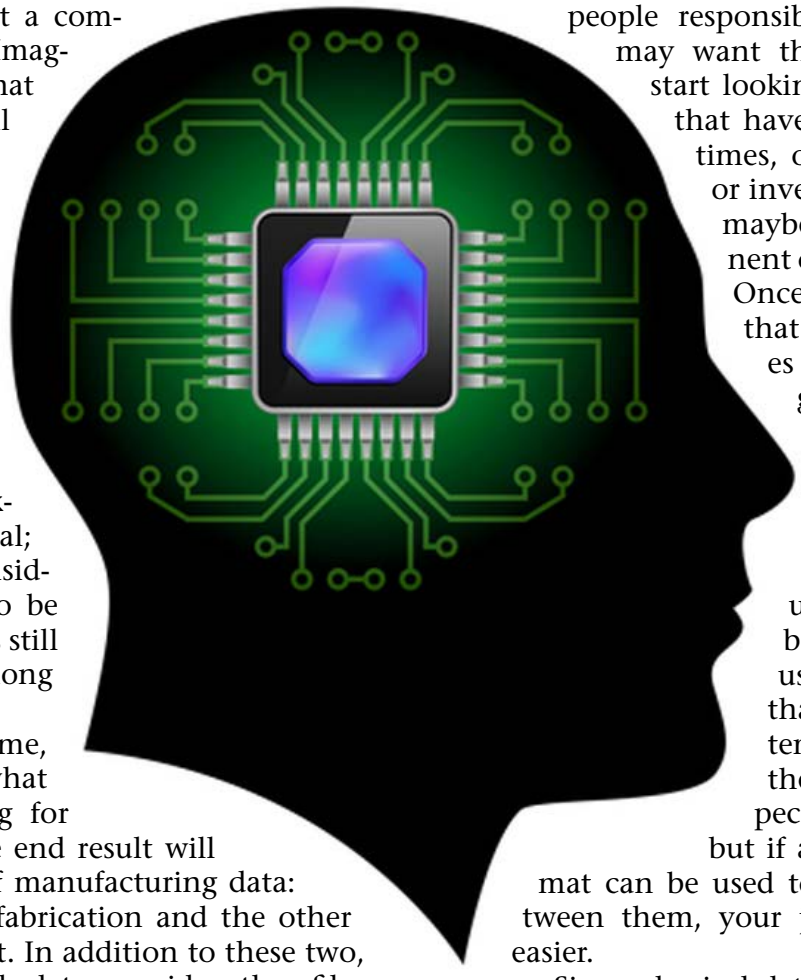
PCB Design Data: What Do Your Customers Expect?

by Jack Olson

SUMMARY: What does a circuit board designer produce? Who are our customers, and what do they expect from us? Here's a brief description of the types of data you will be providing during various stages of the electronics development process.

One vision for the future of our industry is that every CAD system would have the ability to output a common file format. Imagine a single file that could be sent to all of our customers, and each would extract the type of data needed for a specific process. A universal data format for electronics manufacturing will offer many advantages, and many are diligently working toward that goal; however, several considerations still need to be resolved, and there is still no consensus yet among industry leaders.



In the meantime, you need to know what you will be creating for your customers. The end result will be two major sets of manufacturing data: one for bare board fabrication and the other for assembly and test. In addition to these two, you may also be asked to provide other files along the way, so let's take a look at those first.

Bill of Materials (BOM)

When packaging a design, your CAD software will interpret the schematic diagram and map the symbols into components, assigning a unique identifier called a reference designator to each one. Since the system now knows how many of each type of component is required to build the product, a part list or bill of materials (BOM) can be generated.

Even before you start the board layout, several people may be waiting for the BOM information, so don't delay sending it. The people responsible for purchasing may want this information to start looking for components that have long buying lead times, or for cost analysis or inventory control, and maybe even for component obsolescence study. Once you are confident that your BOM matches the design intent, get it to the people who can use it as soon as possible.

Mechanical Data

CAD systems used for circuit board layout are usually different than the CAD systems used to design the mechanical aspects of the product, but if a common file format can be used to transfer data between them, your job may get a lot easier.

Since physical details of the product such as the dimensions of the enclosure or the mounting scheme are most often defined in a mechanical CAD system, it may be easier for a mechanical engineer to define the board outline and send it to you. This process can become quite sophisticated, including the abil-

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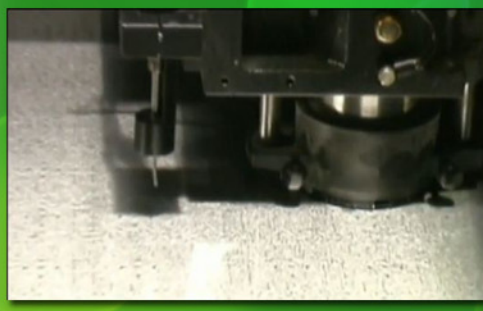

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ity to define keep-out areas, height restrictions, connector locations, mounting hole sizes, etc. Importing this type of data directly into the circuit board layout can save time and reduce the chance for errors and oversights.

If the circuit board layout software can export a file back to the mechanical design software, additional interference checks can be performed before manufacturing begins. Sometimes a 3D model can be created in the mechanical system, and seeing a better representation of your final assembly mounted inside the product can highlight an issue that might not have been apparent in your 2D layout software, so take advantage of it if it is available.

Quoting

Before the design is finished, the purchasing department may ask you in advance for enough information to get a budgetary quote. The fabrication data and drawing will provide everything a bare board fabricator needs to know about the product, but these can't be created before the layout is complete. In the meantime, cost analysis and purchase orders can start if you can provide the basic parameters of the design. For the bare board quote, they will want to know:

- Board size, thickness, and any cut-out or slot requirements.
- Board material including desired final finish.
- Number of layers.
- Approximate number of holes, and smallest hole size.
- Smallest trace width and clearance.
- Quantity of boards and required turnaround time.

Some of these estimates change slightly before the design is finished, but most fabricators are willing to provide a budgetary quote as long as they can adjust the price if there are significant changes.

The Fabrication Data Package

Artwork

You will be providing a description of each layer image either in Gerber format or in one of the other proprietary data formats supported by your CAD system.

Most circuit board artwork is described using the Gerber data format, so I should probably include a little historical background before we move on. The Gerber data format was developed by Gerber Scientific in 1980 as an input to control a photoplotter. A photoplotter was similar to a pen plotter, but instead of using ink on paper it used different sized apertures to expose an image on film, using a beam of light. Each file describes a single layer, and is used to create images for conductive layers, soldermask layers, silkscreen layers, and paste screen layers. These layers were created by flashing exposures in specific locations defined by shape (circles to create plated through-hole pads, for example, or rectangles to create SMT lands, etc.) and connecting them together by drawing exposures from point to point with apertures specified by width (usually round).

When using the original Gerber format (based on a subset of EIA RS-274-D), an aperture list was also required to define the sizes of the draws and flashes, but Gerber data files created using the newer RS-274-X format have the aperture information embedded in each file, so a separate list is not required. Use the newer 274X format if your CAD system can support it.

Although the Gerber data format was developed to control a photoplotter using draws and flashes, modern CAM systems can read in all the data at once and rasterize a complete image for each layer. This is much faster than drawing/flashing each feature sequentially.

Drill Data

Two more types of ASCII files are needed for numerically controlled drilling (NCD). These will be used to define the size and location of all the holes in the circuit board, both plated and unplated.

- A tool table lists the diameter of each drill size and assigns them to tool numbers, and gives instructions about how to interpret the drill data.
- The drill data file contains hole locations for each drill sorted by tool number.

As a supplement to the ASCII drill data files, it is customary to provide additional information related to drilling on the fabrication drawing in the form of a hole legend or drill chart. During quoting, and for quality inspection activities, this summary is easier to read than having to interpret the raw data. Drill sizes are given unique symbols or letters, and the pictorial representation of the board on the drawing will show these symbols as a visual aid.

Netlist

The netlist file is not always included in fabrication data packages, but it probably should be. A bare board can be fabricated without a netlist, but if it is available, an extra level of checking is available that can help ensure that the data files describe the intended connectivity. This file should be in the IPC-D-356 format, which can be created automatically by most PCB layout software packages.

Fabrication Drawing

The fabrication drawing fulfills several important functions to support the circuit board manufacturing process:

- It provides enough information about the design for the bare board fabricator to prepare a quote.
- It adds all the extra details about the build that aren't easily incorporated into the data files, like material and final finish.
- It lists the criteria by which the finished product will be evaluated for acceptability.
- It serves as a tool to be used during final inspection.
- It is a record or document to store the history of a product by title, part number and revision, physical dimensions, and lists the name of the designer and possibly several other supporting entities as well as the company name and address, etc.

Several different types of information can be found on a typical fabrication drawing: board details including layer stack-up and construction, materials and process specifications, conductor width and clearance minimums, fabrication allowances, impedance requirements, marking requirements, test coupon requirements, performance requirements, and a graphical representation of the board with critical dimensions.

> ***As a supplement to the ASCII drill data files, it is customary to provide additional information related to drilling on the fabrication drawing in the form of a hole legend or drill chart.***

ReadMe.txt

Including this file into your data package gives you an opportunity to add extra information to the bare board fabrication order. For example, you may have intentionally shorted two nets together (like AGND and DGND) and you don't want the fabricator to put your job "ON HOLD" because of a netlist discrepancy. A README.TXT file is the place to include additional notes that you may not want to show in the final documentation. This is also a good place to list yourself or someone else as a contact, with name, phone number and e-mail address.

The Assembly/Test Data Package

Assembly Drawing

The centerpiece of an assembly drawing is a pictorial representation of what the finished electronic assembly will look like. The graphics should clarify component polarity, and provide other details specific to the assembly. Notes can be added for any special instructions and to indicate what level of workmanship and acceptability is expected.

Solder Paste Data

If surface mount components are used in the design, they will be attached to the board using solder paste. This solder paste is applied to the surface of the board using a stainless steel paste screen, which is typically created using a Gerber data file that describes the areas of the

PCB DESIGN DATA: WHAT DO YOUR CUSTOMERS EXPECT? *continues*

board where paste is needed. Two paste screens are required if there will be surface mount parts on both sides of the board assembly.

Paste screen technology is quite sophisticated, and unless you really know what you're doing, you should provide paste screen apertures that are the same size as the lands you will be soldering to. This will give the paste screen manufacturer a known starting place to begin making modifications for various technologies.

Component Placement Data

Components needed for the assembly are purchased in quantity, loaded onto reels or inserted into plastic tubes. A component pick-and-place machine features a specific number of feeders that are loaded with these tubes and reels. After solder paste is applied to the land patterns of a bare board, it is loaded into the pick-and-place machine where a camera aligns the board using metal targets called fiducials (usually round dots 1 mm in diameter etched into the surface conductor layer). Then components are picked up one at a time and placed on the board in specific locations, at the proper rotation. An ASCII data file contains the fiducial locations, and the X-Y coordinates and rotation for each component.

ReadMe.txt

This is the place to include additional notes that you may not want to show in the final documentation. This is also a good place to list yourself or someone else as a contact, with name, phone number and e-mail address.

Test Data

Some products will be manufactured in a high enough volume to make the expense of an in-circuit test (ICT) fixture worthwhile. An ICT fixture and program will be developed to test the final assembled circuit board before it is mounted into the product. For these products you will add test points to the board layout, and then generate an extra file containing the test point coordinates. Many CAD systems can help automate this task. A copy of the schematic may also be helpful for the person developing the test program.

Compressed Archives

Data files are often combined and compressed into a single file called an archive, using a file extension such as ZIP, RAR or TAR. The resulting archive file can be transferred between customers and suppliers, and the individual files can be easily restored at the destination. Three of the most important advantages of compressed archives are:

- Compressed archives keep necessary components of a package together, making organization easier and reducing the chance of missing files.
- Compressed files are much smaller, needing less storage space, less time and less network usage for transfers.
- The software that compresses and uncompresses archives has automatic built-in error checking.

Unless your CAD system can output a single file format that is supported by your manufacturing process, you will probably be combining several different types of data into ZIP files before sending them out to your manufacturing partners.

Milestones

Throughout the design process there will be several different people using your data. After you work through a few designs, start recording the steps that you did to get from start to finish, and who needed what along the way. Then rearrange the steps where possible to get the data to the people who need it as soon as possible. You don't want to create bottlenecks for others, and it's better for you to be waiting on them than it is for them to be waiting on you. **PCBDESIGN**

Jack Olson, C.I.D.+, has been designing circuit boards full-time for more than 20 years. He would like to thank all the friends and colleagues who have taken time to teach him about the real world of electronics development.

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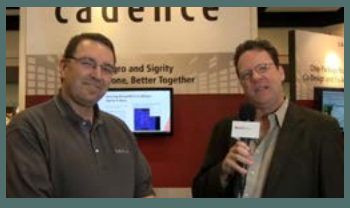

Brad Griffin, product marketing director for Cadence Design Systems, discusses the company's acquisition of Sigrity, as well as the fairly seamless blending of the two companies' cultures.

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2013 DesignVision Award Winners Recognize Innovation

UBM Tech has announced the names of the 2013 DesignVision Award winners, including industry firms Mentor Graphics, TE Connectivity, ANSYS Inc., Upverter, MicroSemi, Teledyne LeCroy and Averna. DesignCon evaluated products from hundreds of exhibitors to choose the winners, who were recognized at an awards ceremony at DesignCon 2013 in Santa Clara, California.

Winners were selected based on three criteria: how well the product met the market's vision and offered unique insight into customer needs; the originality of the solution and if it offered a new approach to meeting market needs; and the quality of the implementation and how well it fits the market requirements.

The 2013 DesignVision winners by product category are:

- Mentor Graphics, Tessent IJTAG - IC Design Tools Category
- TE Connectivity, STRADA Whisper - Interconnect Technologies and Components Category
- ANSYS Inc., HFSS (for ECAD with Cadence) - Modeling and Simulation Tools Category
- Upverter, Upverter - PCB Design Tools Category
- MicroSemi, SmartFusion2 - Semiconductor Components and ICs Category
- Teledyne LeCroy, HDO High Definition Oscilloscopes - Test & Measurement Category
- Averna, Proligent Analytics 6.0 - Verification Tools Category

"We had quite a challenging time choosing these winners among all of the innovative products we judged," said Patrick Mannion, Content Director and Brand Director EDN, Test & Measurement World & Planet Analog. "Ultimately, our 2013 winners represent the best of the best in each of their respective industries."

Postmortem Simulation

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

SUMMARY: Developing the practice of performing a postmortem analysis on every project facilitates a culture of continuous improvement. This embedded culture of ongoing, positive change is the best way to ensure long-term success.

Often we find that PCB simulation is engaged too late in the design cycle. This results in the simulation process becoming more a post-mortem to uncover what has gone wrong with the design and how it can be resurrected to work as intended.

In my work as a high-speed analyst, I sometimes get called on to fix problems that could have been prevented. However, a total disaster can usually be avoided and final success achieved (providing the conceptual design has been validated).

Ideally, every high-speed design should be exposed to the preventative medicine of pre-layout simulation and proactive stackup and power-delivery optimization.

As with any forensic postmortem, a thorough external examination is undertaken to see if there are any visible signs of impairment that may identify the cause of the problem. This is what I refer to as "eyeballing" the design. It is actually amazing what can be picked up just by looking closely at the PCB database. I think we have all experienced the case where we simply cannot see the obvious because we are intimately involved in the design – that is, our subconscious does not warrant rechecking the obvious. That is why I always advocate having a second, equally qualified person thoroughly check a PCB before handover to manufacturing.

The following is a short list of issues to regularly check in a design:

- Minimum edge/tooling hole clearances and component to edge of board clearance.
- Thermal reliefs are not compromised.
- Split planes (if present) are correctly placed.
- No critical nets cross split planes.
- No critical (high-speed) nets in the analog areas.
- Critical nets must not change reference planes unless accompanied by a stitching via or bypass capacitor.
- Matched length signals – memory data, strobe, clock, address, control and command signals are routed to specs.
- All critical nets are buried between solid planes. The allowable length of the exposed portion of a critical net is limited.
- All critical nets must be routed with adequate clearance to avoid crosstalk.
- All power and ground traces longer than 500 mils must be wide enough to carry the specified current.

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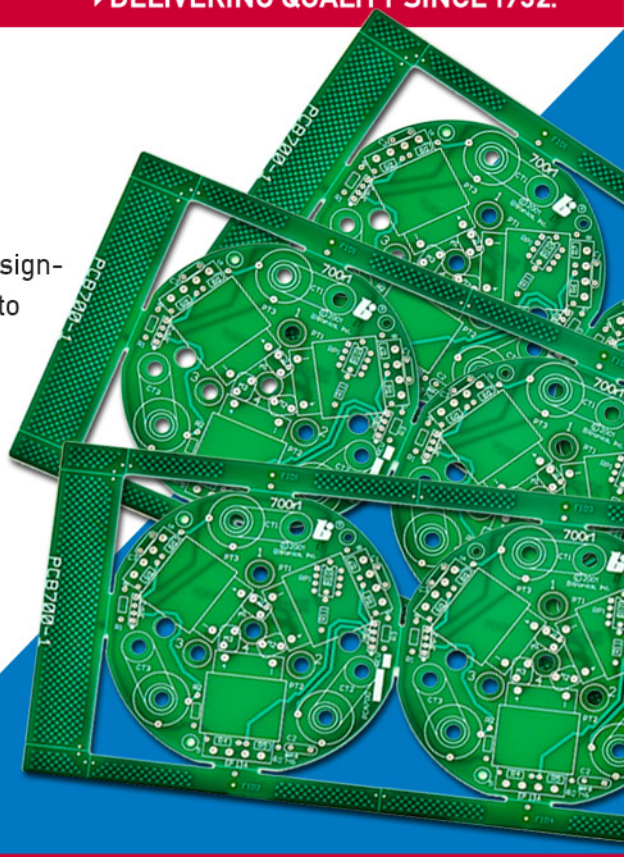

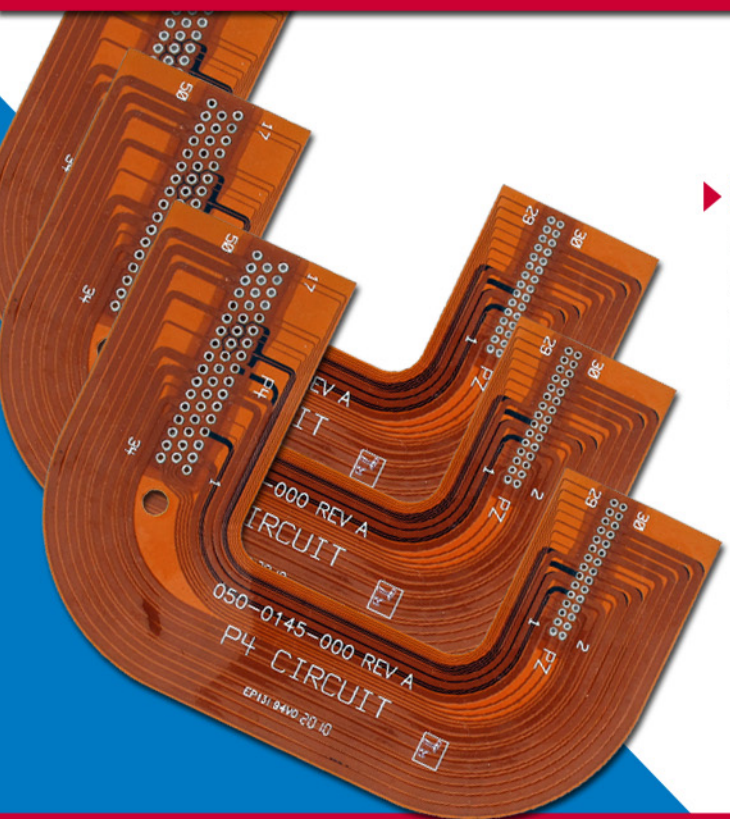

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- All oscillators must be placed within 500 mils from the clock driver.
- Critical nets are not within 3x trace width of the edge of their reference plane.
- Decoupling capacitors are placed within 500 mils from each IC power pin.
- The trace connecting between a decoupling capacitor to the associated via to the power/ground reference plane must be no longer than 200 mils and be 20 mils wide.

Of course, there are many more rules embedded in the experienced designer's head. A digital simulator may also pick up some of these rule violations, but software automation is not a surrogate for good design judgment, and doing forensics on your own designs.

Next, the examiner takes a look inside at the major organs – the PCB stackup and power distribution networks (PDN) in this case.

A poorly designed substrate, with inappropriately selected materials, can degrade the electrical performance of signal transmission, increasing emissions and crosstalk, and it can also make the product more susceptible to external noise. These issues can cause intermittent operation, due to timing glitches, and interference dramatically reducing the product's performance and long term reliability.

The less than desirable stackup in Figure 2 can be exported from Altium Designer (S09 to R13) into the ICD Stackup Planner to incorporate dielectric materials and adjust the stackup for optimal performance. The stackup is then modified to give 50 ohms single-ended and 100 ohms differential impedance by moving the plane layers and adding dielectric materials from the Stackup Planner's dielectric materials library.

Once modified, the stackup in Figure 3 can then be exported back to Altium Designer to also include impedance-controlled routing and differential rules. Plus, the stackup can also be exported to HyperLynx LineSim for pre-layout analysis, BoardSim for post-layout analysis, PADS and Allegro.

To promote communication with PCB fabricators, an Excel spreadsheet output (Figure 4)

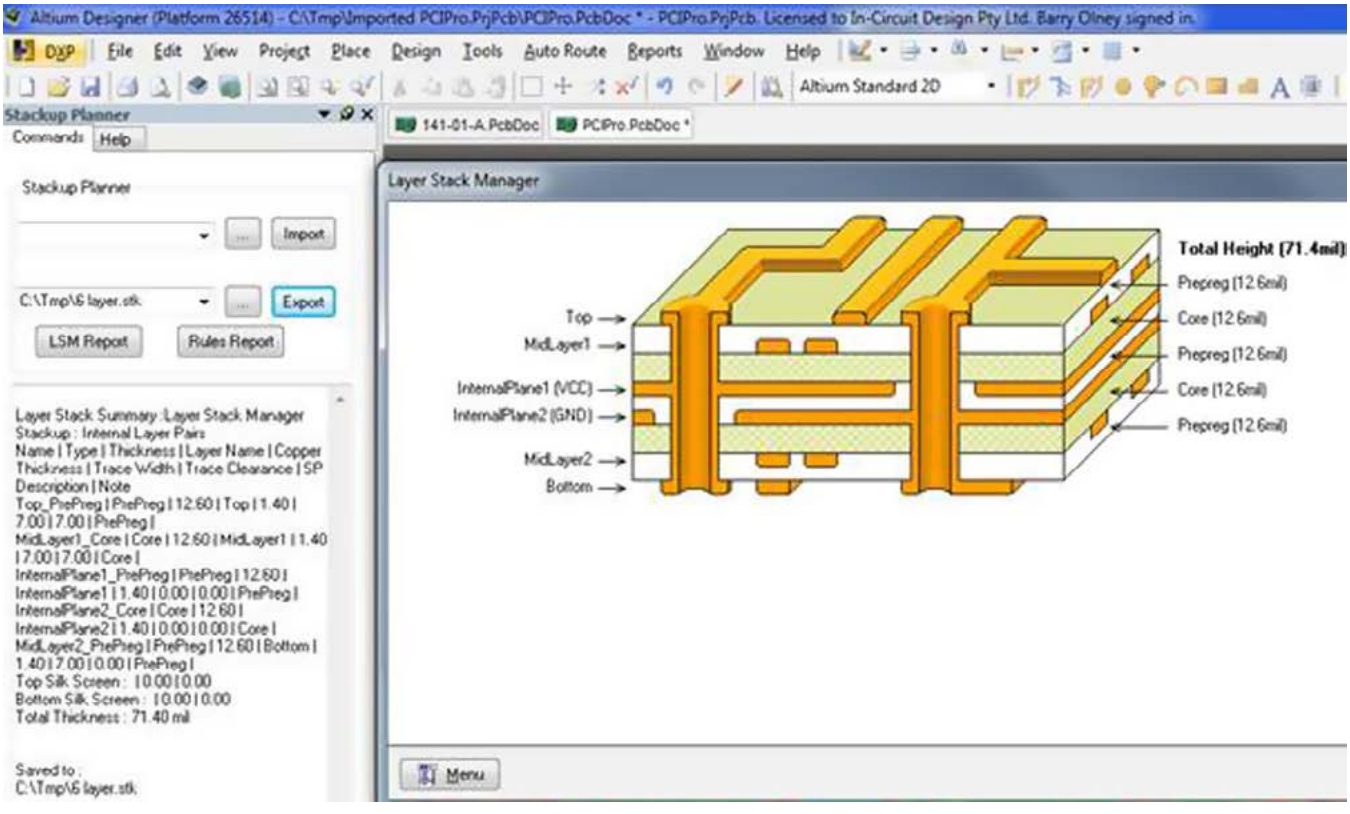


Figure 2: Exporting the stackup from Altium Designer's layer stack manager.

is also available from the ICD Stackup Planner. It is for this reason that the ICD (.stk) format is fast becoming the industry standard for impedance controlled data collaboration between engineers, designers and fabricators.

If the product is showing "flakiness" in functional tests, or even in production, the cause may involve inadequate PDN design. Ideally,

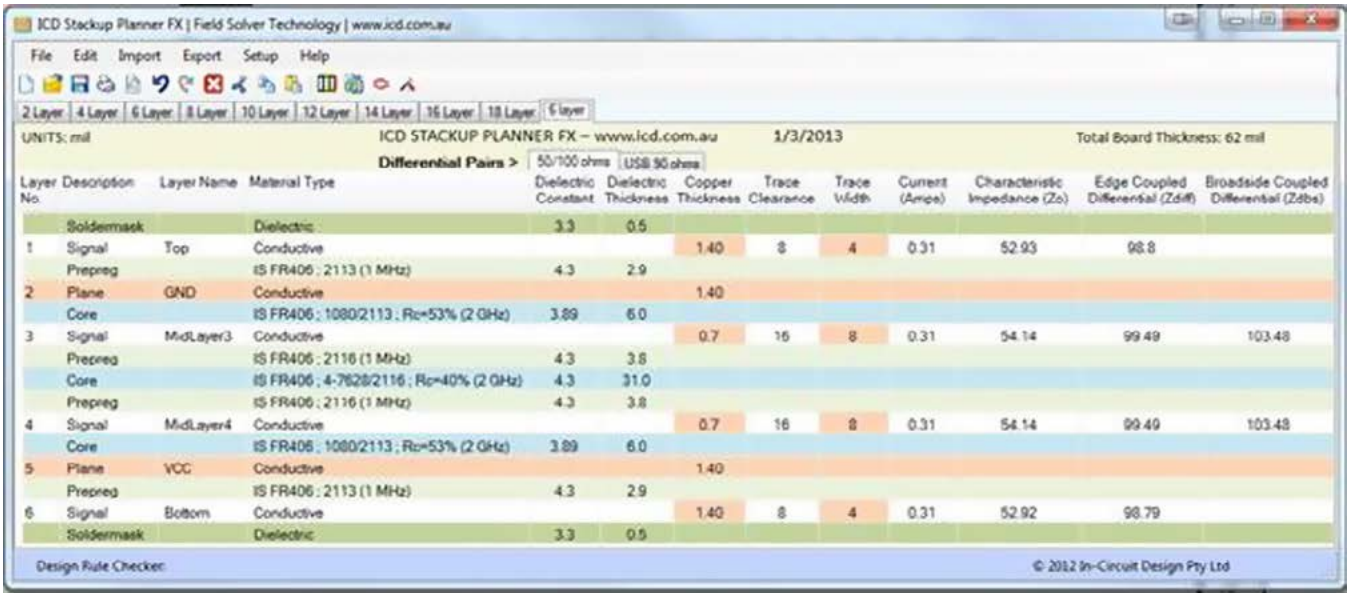


Figure 3: The modified stackup can be exported from the ICD Stackup Planner back to Altium Designer.

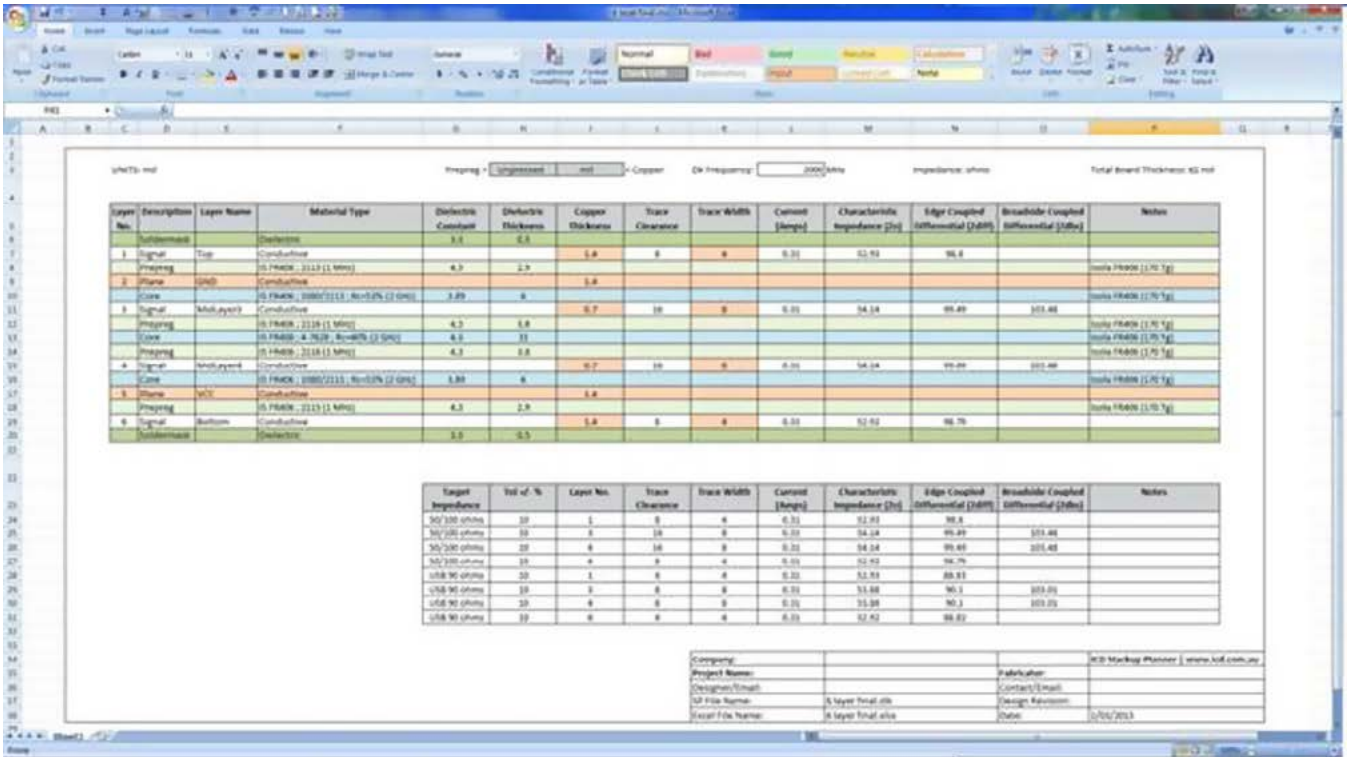


Figure 4: The stackup, exported to Excel, allows engineers and PCB designers to communicate more effectively with fabricators.

POSTMORTEM SIMULATION *continues*

issues like this should be resolved before a single chip has been placed on the board.

Decoupling capacitors supply instantaneous current (at different frequencies) to the drivers until the power supply can respond. In other words, it takes a finite time for current to flow from the power supply circuit (whether on-board or remote), due to the inductance of the trace, and/or leads to the drivers. Every decoupling capacitor has an equivalent series inductance (ESL), causing its impedance to increase at high frequencies. In order to reduce this inductance, a number of small-value decaps can be placed in parallel, as close as possible to each power pin using a thick, short trace or – even better – directly to the low-inductance plane.

The selection of capacitors, with the correct attributes, is a trial and error process and needs to be done with the assistance of an analysis tool. The ICD PDN Planner (available for download from www.icd.com.au) illustrates a typical decoupling scheme in Figure 5.

In a postmortem, blood tests are also sent to pathology to be analyzed. This gives the pathologist a few clues regarding systemic issues that might escape initial observation. In my mind, this is analogous to whole-board analysis, with a simulator like Mentor Graphics HyperLynx. Batch simulation flags signal integrity, crosstalk, timing, and EMC hot spots across the entire design. Default IC characteristics, crosstalk of 150mV maximum and EMC to FCC, CISPR Class A and B are setup in the simulator.

The post-layout simulation analysis is an extensive interactive board level simulation that takes the analysis to the next level, simulating trouble spots identified by the batch analysis in order to further resolve the issues with greater accuracy. The virtual oscilloscope and spectrum analyser give the examiner another view, similar to the images of an MRI and X-ray films which allow the examiner to visualize internal trauma and minute fractures. The simulations allow in-depth analysis of signal integrity and crosstalk within the substrate.

Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer but may also be broadside-coupled from the adjacent layer. It is for this reason that orthogonal routing is recommended on adja-

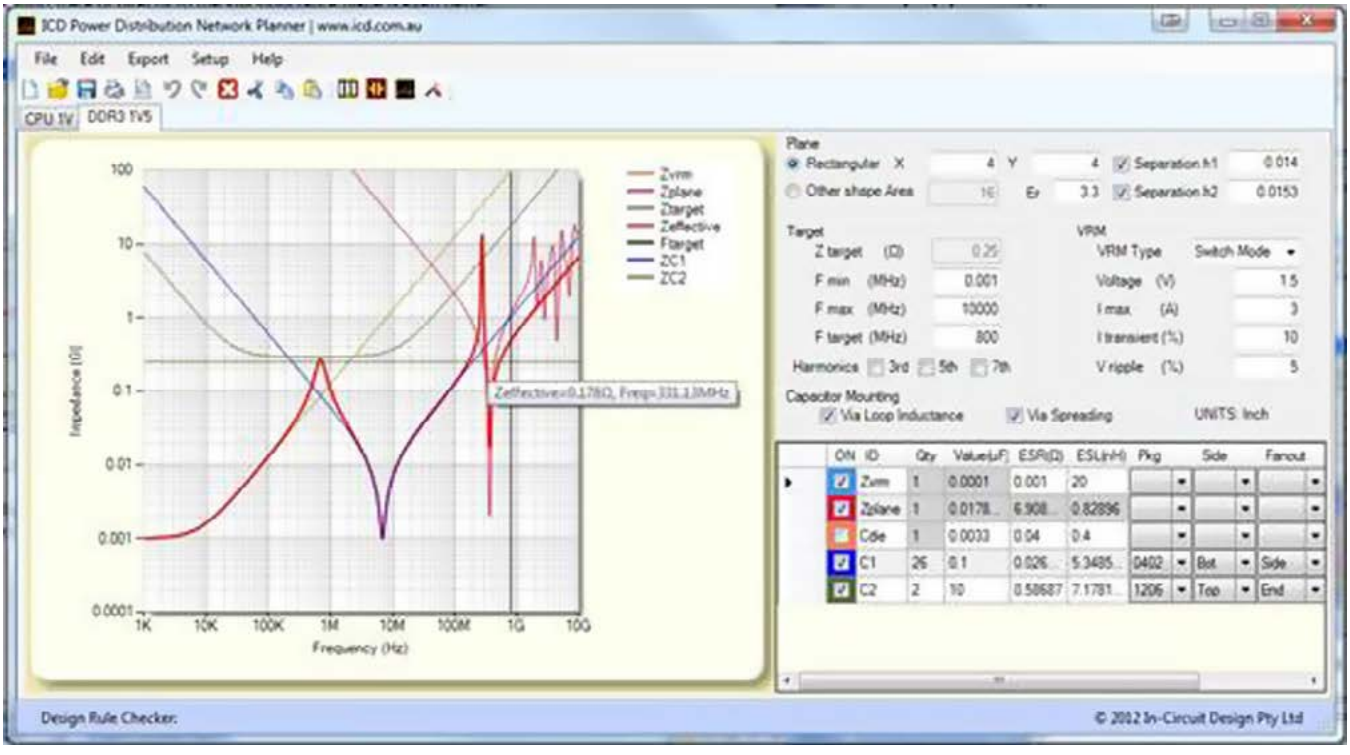


Figure 5: The ICD PDN Planner illustrates a typical decoupling scheme for 1.5V DDR3 supply.

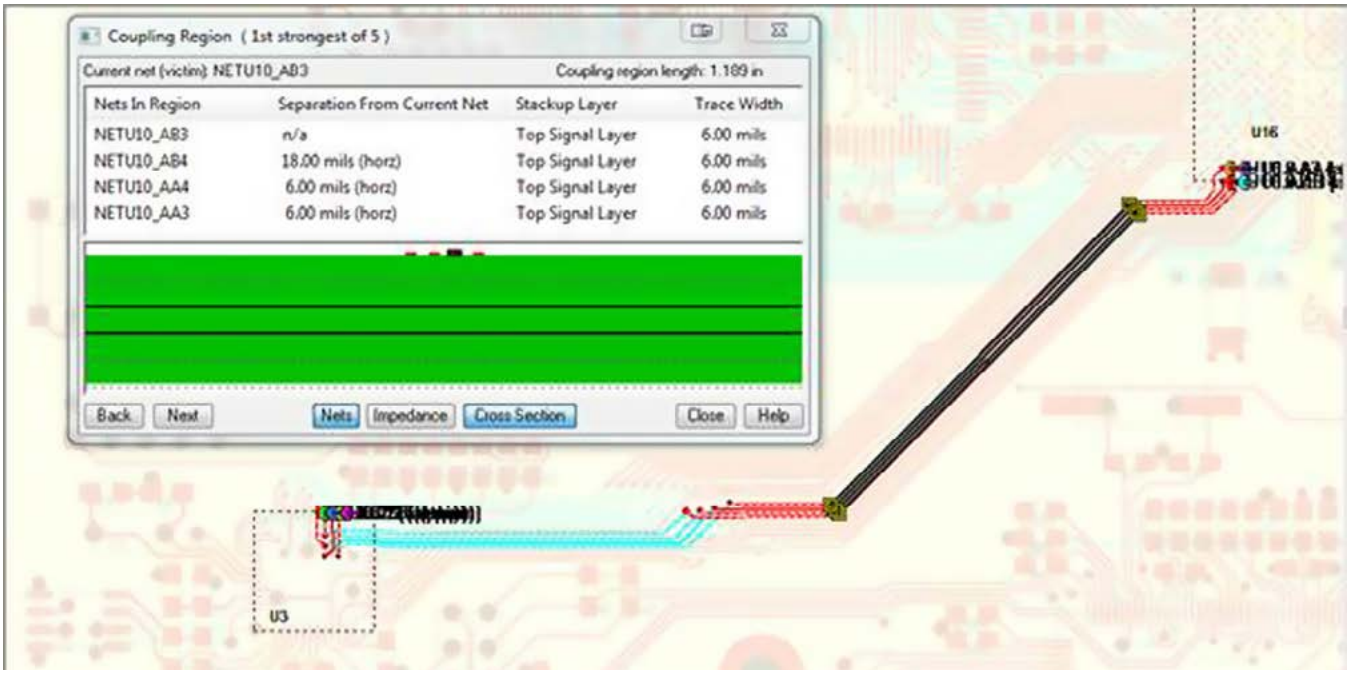


Figure 6: HyperLynx shows crosstalk on manually routed parallel traces segments.

cent layers (between planes) to minimize the coupling area. Figure 6 shows this crosstalk on the 45-degree routes. It is recommend that segments are only routed to a maximum of 500 mils in parallel or that the clearance is increased to at least 3x trace width to avoid coupling.

The next step in the analysis is to examine timing: This is the heartbeat of the design. Irregular heartbeat can have catastrophic affects just as irregular timing can cause intermittent faults in a digital system. In the classic high-speed design flow, timing specifications and simulation results are compared to check skew and set and hold times to ensure everything is operating like clockwork.

Figure 7 illustrates the timing of the clock compared to the address, control and command signals of a DRR3 memory design. The skew can be up to 200ps for

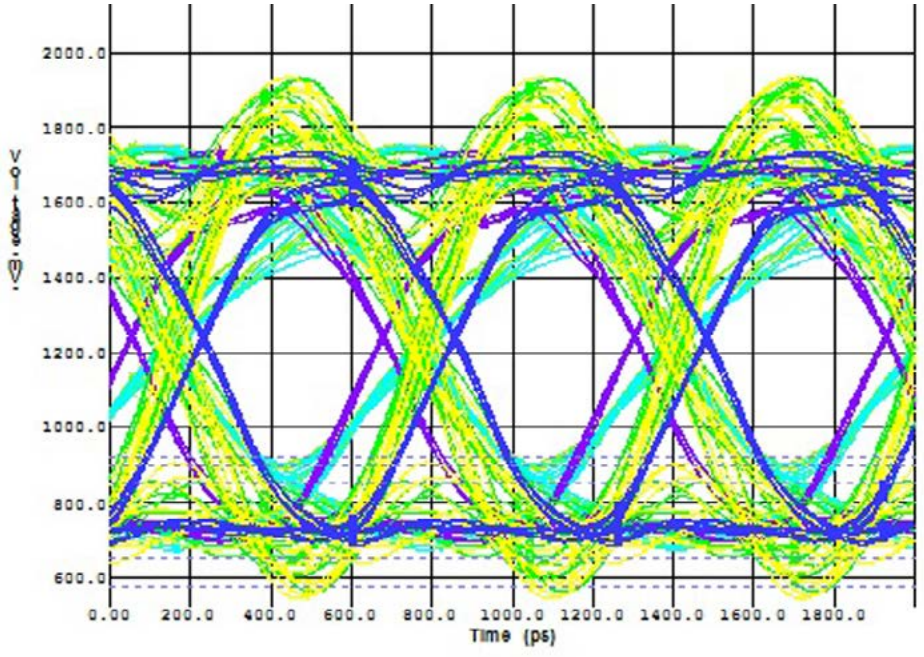


Figure 7: Skew of clock to address, control and command signals of DDR3 memory.

DDR3-800. Also, the skew between data lanes and data strobes should be kept to less than 125ps and the eyes should be wide open. DDR3 is much easier to route, in fact, than DDR2 as leveling can be used to synchronize the delay of groups of signals. All critical signals are checked with the physical information that is obtained from the PCB data base (e.g., trace lengths, clearances, vias, etc.) to ensure that the design complies to specification.

Conclusion

Developing the practice of performing a postmortem analysis on every project – identifying both the good and the bad – facilitates a culture of continuous improvement. Embedding a culture of ongoing, positive change inside a project delivery organization is the best way to ensure long-term success. Postmortems are an important link in this chain of positive improvement.

Points to remember:

1. Ideally, the simulation should be done during the design process to ensure design integrity.

2. A postmortem should be performed on every project, creating a culture of continuous improvement.

3. For a project that suffers from intermittent flakiness, the postmortem can begin with a thorough external examination – a second set of eyeballs – looking for the obvious.

4. The PCB stackup can be the source of problems that include impedance mismatches, signal integrity problems, crosstalk, or emissions. As part of the stackup optimization process, a PCB stackup can be exported from several PCB environments to the ICD Stackup Planner to incorporate dielectric materials and adjust the stackup for optimal performance.

5. Once modified, the stackup can then be exported back to the PCB environment or to HyperLynx for signal integrity, crosstalk, and EMC analysis. With Altium Designer, impedance and differential routing rules can also be incorporated into the export.

6. To improve communications with PCB Fabricators, an Excel spreadsheet output is also available.

7. The design of the PDN is another important part of the conceptual design process, and should be analyzed as part of a comprehensive postmortem, as well.

8. Post-layout (board-level) analysis can find systemic trouble spots in a design.

9. Crosstalk is typically picked up on long parallel trace segments.

10. Interactive simulation takes the investigation process deeper, including detailed signal integrity analysis, as well as crosstalk and timing.

11. Timing is the heartbeat of the design. Irregular timing can cause intermittent faults in a digital system. **PCBDESIGN**

References

1. Advanced Design for SMT – Barry Olney

2. Beyond Design: Interactive Placement and Routing Strategies – Barry Olney

3. Beyond Design: Intro to Board-Level Simulation and the PCB Design Process – Barry Olney

4. Beyond Design: Mixed Digital-Analog Technologies – Barry Olney

5. PCB Design Techniques for DDR, DDR2 & DDR3, Part 2 – Barry Olney

6. PCB Design Techniques for DDR, DDR2 & DDR3, Part 1 – Barry Olney

7. The ICD Stackup and PDN Planner can be downloaded from www.icd.com.au

Barry Olney is the managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, and is a PCB design service bureau that specializes in board-level simulation.

Most-Read PCB007 News Highlights

Exception's PCB Solutions Business Acquired by Fastprint

Qiu Xingya, chairman of Fastprint, says, "This acquisition will help Fastprint establish a strong base in Europe for both manufacturing and trading. Post-acquisition, we will continue to invest in PCB manufacturing to maintain, as well as enhance, the market-leading position in Europe in terms of quality and speed."

Global PCB Market to Reach $68.5B in 2016

Asia growth will be sustained mainly by domestic demand but will nevertheless experience a very respectable average annual growth of a little less than 5% in 2013 before picking up in 2015 resulting in a growth rate of between 6% and 7% for China between 2011 and 2016. Global PCB market value will increase from $56.6 billion in 2011 to $68.5 billion in 2016 meaning China's share of PCB production will increase further from 45% to 51%.

N.A. PCB Industry Reports Negative November Results

Rigid PCB shipments were down 5.4% in November 2012 from November 2011, and bookings decreased 8.7% year over year. Year to date, rigid PCB shipments declined 4.5% and bookings decreased 0.9%. Compared to the previous month, rigid PCB shipments were down 5.6% and rigid bookings fell 2.1%. The book-to-bill ratio for the North American rigid PCB industry in November 2012 fell to 0.95.

TTM Partners in EU Optical Transmission Technologies

TTM Technologies, Inc. is partnering in a development project of optical data transmission technologies sponsored by the European Union. The EU is providing EUR 9 million funding for the four-year project, which began in October 2012 under the name PhoxTroT.

Viasystems' PCB Segment Expects Sales Drop in Q4

"Despite reduced sales and production levels in our fourth quarter, we estimate that we were successful in managing our costs to stabilize our gross margins as a percent of sales at a level consistent with our third quarter result," said David M. Sindelar, CEO.

IPC Releases Annual Report; Much Accomplished in 2012

Last year proved to be a year of modest growth for the electronic interconnect industry. It was also a year filled with innovative standards development, a flurry of environmental and governmental legislation, global activity expansion, membership service initiatives, and more.

IPC Strengthens Support for Chinese Manufacturers

China's rise as a manufacturing powerhouse is one of the inescapable factors in any analysis of the electronics industry. With a powerhouse of its own, new IPC China President Philip S. Carmichael, IPC is beefing up its efforts to help Chinese manufacturers come into alignment with other global companies that employ IPC standards to improve business plans and manufacturing capabilities.

Q.P.I. Group Acquires Macer Sweden AB

The Helmond based company Q.P.I. Group Holding B.V. has acquired the Swedish company Macer Sweden AB, which specialises in the supply of printed circuit boards and in DFM (Design For Manufacturing).

Invotec Appoints Mark Sykes Sales Account Manager

Matt Bowman, sales director, commented, "We are delighted to announce the appointment of Mark Sykes as account manager, focusing on building on our client base in the Southern region. Mark brings plenty of experience and the drive our clients demand."

Spirit Circuits Appoints Harzendetter as Sales Agent

Spirit Circuits has appointed a new sales agent Rupert Harzendetter to handle operations in Germany.

Efficient Simulation Using High-Frequency Printed Circuit Materials

by John Coonrod
ROGERS CORPORATION

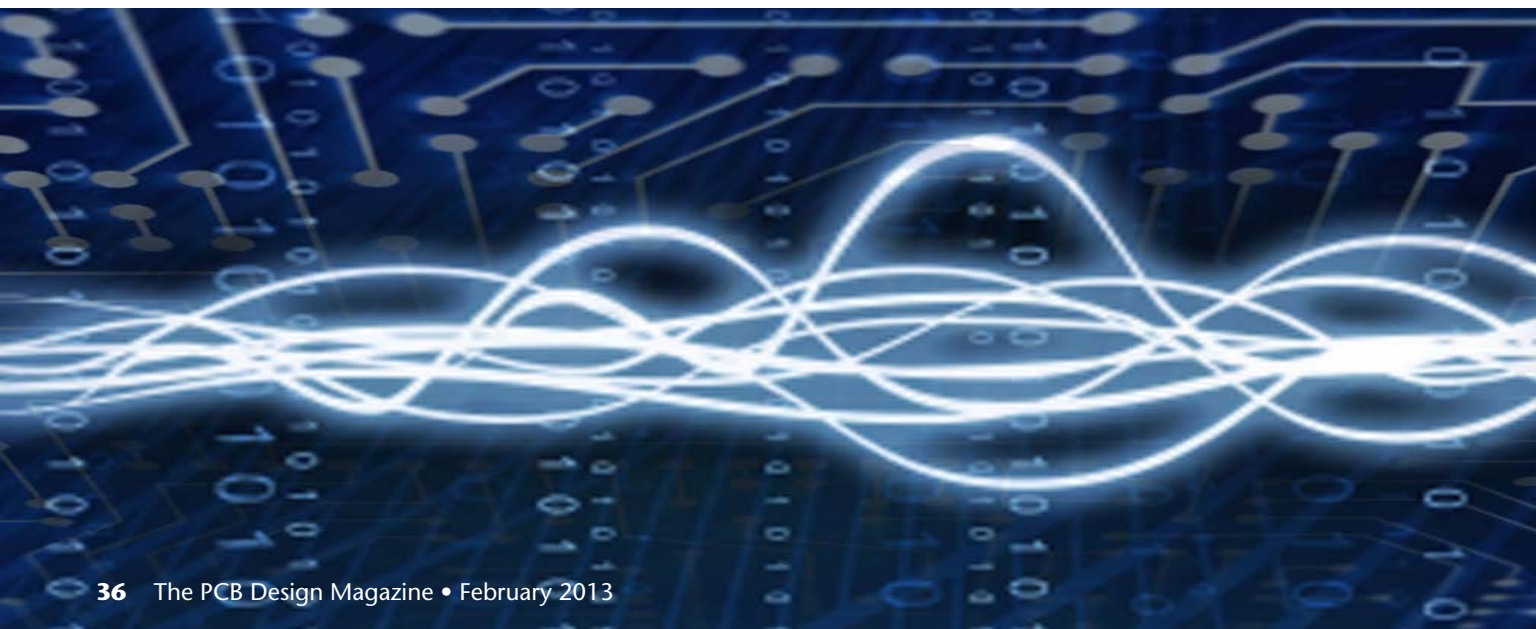
SUMMARY: ***Many different types of circuit simulation software are available, and each one is tailored to meet a different need. Dielectric constant and dissipation factor are two of the more important substrate properties to consider during simulation. The Dk value is provided on material datasheets, but Dk value can vary substantially depending on the test method.***

The general type of simulation software most often used for high-frequency laminates is impedance modeling or electromagnetic modeling tools. These software tools all require that circuit geometry be input, such as the conductor thickness, width, substrate thickness, and other details. The substrate properties which are generally most important are the dielectric constant (Dk or ε_r) and dissipation factor.

The Dk value is provided on material datasheets; however, anyone who is less savvy with material issues may be unaware that the Dk value can be very different depending on the test method. If the test method is not the same configuration as the circuit the designer is concerned with, the Dk value may be less accurate. A simple example: A common test method used for high-frequency circuit materials is the clamped stripline resonator at 10 GHz. If the designer is using this material and concerned with a microstrip transmission line circuit operating at 2 GHz, the Dk data from the stripline resonator may not be as accurate as needed.

The different test methods are designed for specific reasons. The clamped stripline test method is a very good test method for evaluating raw substrate properties at a specific frequency and in a relatively high-volume testing environment. The stripline structure has a layering configuration of ground-signal-ground and this test method uses a clamping fixture that can test raw substrate quickly. The test uses a thin circuit (signal layer) which features the copper resonator pattern. On both sides of this circuit, the raw substrate will be placed and then the outer metal plates (ground planes) will be clamped together. The Dk can be tested within a few minutes, and when a materials manufacturer requires testing several hundred substrate samples per day, this is a good test method to use.

Referring back to the example, where stripline and microstrip were compared, the mi-



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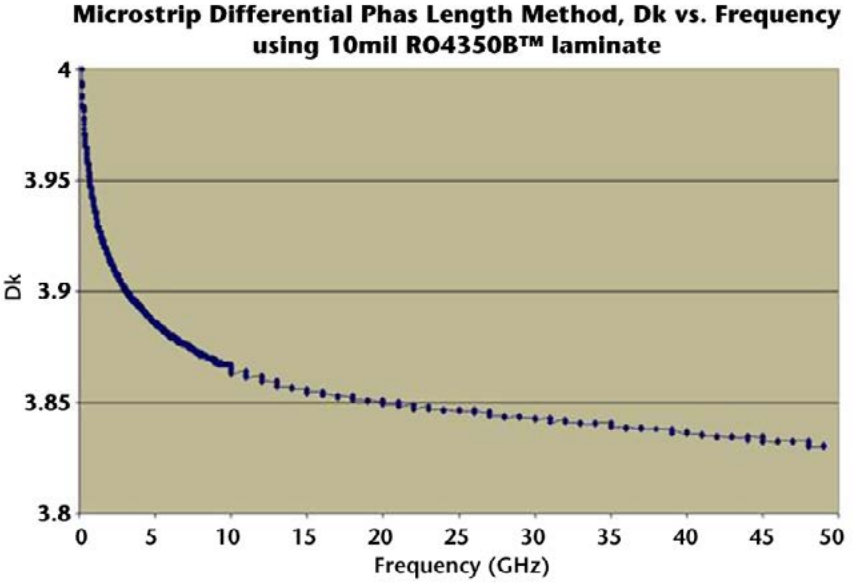

Figure 1: Graph showing Dk vs. frequency curve.

crostrip circuit is a two-copper-layer circuit with a layer configuration of signal-ground. This is obviously very different from the stripline structure, and one apparent difference is that the microstrip will have some electric fields in air while the stripline will fully contain all electric fields within the substrate. This difference by itself shows how data collected for a stripline structure may be different than for a microstrip circuit. Another possible issue is that the Dk of any circuit material is frequency dependent. The variance of the Dk as compared to frequency is called dispersion, and some circuit materials have more dispersion than others. Most high-frequency circuit materials have relatively low dispersion, which means the Dk doesn't vary much with frequency. The stripline resonator is testing the substrate at a specific frequency and in many applications the frequency of concern will be different than the test method frequency. Many other applications may be wideband where the Dk performance over a wide range of frequencies can be important to know.

Most circuit material suppliers understand the different test methods and the need for knowing the Dk at different frequencies and for different circuit structures. Rogers Corporation can provide design Dk data in order to assist in circuit design with high-frequency circuit materials. The majority of Dk testing is done on microstrip transmission line circuits. The test method used is the microstrip differential phase length method which uses circuits made on the same sheet of material, which are identical in every manner except length. There is a long circuit and a short circuit. The testing process nearly eliminates the effects of the connectors and signal launch, and generates data specific to the circuit and materials. The data yielded from this test is a Dk vs. frequency curve as shown in Figure 1.

A curve like this can be very helpful for circuit designers concerned with Dk at varying frequency ranges. This curve also shows something true of all circuit materials at lower microwave frequency (less than 8 GHz). The Dk vs. frequency response is non-linear. This area can have a different trend for dissimilar materials with different Dk, dissipation factor, thickness and sometimes copper type.

The high-frequency circuit material suppliers typically possess an abundance of information regarding their materials used in different circuit configurations as well as frequency. It is always recommended to get the material supplier involved with new applications in order to help minimize potential issues. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division. About half of his 25 years of professional experience has been in the flexible PCB industry doing circuit design, applications, processing and materials engineering. He has also supported high-frequency, rigid PCB materials for Rogers for the past 10 years. Coonrod may be reached at john.coonrod@rogerscorporation.com.

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Welcome

to the 2013 IPC APEX EXPO Show Guide

You'll find more than 50 countries represented at the industry's premier event this year, held once again at the San Diego Convention Center, on the waterfront in downtown San Diego. Featuring advanced and emerging technologies in printed board design and manufacturing, electronics assembly, test and printed electronics, APEX is a great place to find new suppliers with new solutions and connect with colleagues from around the world, plus there are plenty of free offerings. Click here for a complete show guide.

Just a few highlights of what attendees may expect include:

- FREE! More than 400 exhibitors showing equipment, materials and services for printed boards and electronics manufacturing—plus printed electronics! There's no better place to see and compare

- The largest technical conference for our industry in the world. Highly selective, the conference presents new research and innovations from experts in the fields of electronics assembly, test and board fabrication and design

- FREE! Industry poster sessions—Catch up on the latest research and meet the authors
- Professional development courses provide comprehensive updates on pressing industry concerns

- Standards development meetings that help shape the future of our industry.

- IPC International Hand Soldering Grand Championship—Compete in or watch the excitement on the show floor

- On the show floor, view cutting-edge products and services in the New Product Corridor; get support on cleaning and contamination monitoring at the Printed Board Assembly Cleaning and Contamination Testing Center Live; and check out informational resources at the IPC Bookstore

- Networking opportunities including an International Reception, First-Timers' Welcome, IPC Tech Talk, Women in Electronics Networking Meeting, and IPC Government Relations Committee Open Forum allow attendees to meet colleagues, get updates on key issues and share ideas

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IPC APEX EXPO Free Keynote Addresses—*All Three Days!*

Opening Keynote Address:
Tuesday, February 19, 8:30-9:30 a.m.

Michio Kaku, Ph.D.

Imagine, and Create, the Future

Join theoretical physicist, best-selling author and futurist Dr. Michio Kaku for an awe-inspiring look at the future! Dr. Kaku is an internationally recognized authority on Einstein's unified field theory and known for using science to predict trends affecting business, commerce and finance.

Dr. Kaku's keynote will present a vision of life in the year 2100, culled from ideas of 300 of the country's most influential scientists. He will explore revolutionary advancements in medicine, energy production, artificial intelligence and aeronautics that will forever change our way of life.

"Electronics has completely revolutionized our world over the past 50 years. Your industry is a critical building block for future advancement, and it is my great pleasure to share my research and predictions with you."

Let yourself be drawn into a future where innovations like Internet-enabled contact lenses let you surf the Web with the blink of an eye… where your commute to work is stress-free, because your car drives itself while you relax…and where tiny brain sensors let you move objects using only the power of your mind. Don't miss this wild and inspirational ride into the future with Dr. Kaku!

Dr. Kaku is one of the world's most widely recognized figures in science. His television documentaries for the BBC, and Science and Discovery channels, as well as his radio shows, such as Science Fantastic, and his New York Times best-selling books like Physics of the Future have popularized science and roused the interest of millions of followers around the globe. A prolific writer, Dr. Kaku has also authored articles for scores of publications ranging from major-market newspapers to popular business, computer and science magazines.

Following his keynote, Dr. Kaku will sign copies of his latest book, Physics of the Future, which will be available for purchase on-site.

Day Two Keynote Address:
Wednesday, February 20, 8:00-9:00 a.m.

Dr. Larry Burns

Reinventing the Automobile

Can you imagine driverless cars?

According to Dr. Burns, former corporate vice president of research & development and strategic planning at General Motors, some of the transformational technology needed is only five to ten years away from being mass-produced. Speaking from 30 years of experience with GM, along with his new pursuits as a director of the Program on Sustainable Mobility for The Earth Institute at Columbia University; a consultant for Google's pioneering self-driving car program; a contractor with National Renewable Energy Laboratory; and a professor of engineering practice, industrial and operations engineering at the University of Michigan, Dr. Burns will

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I had mentioned to you upon your last visit that Prototron should feel free to use SelfCharge Inc. as a reference. I believe I speak for everyone in our organization when I say that Prototron has been and continues to be an integral part of SelfCharge's product development. Prototron has had an impeccable ability to meet our high quality standards, on-time delivery performance and price targets.

Thank you for the continued support. We are looking forward to a long and prosperous business relationship.

Brady L. Boyd, C.P.M.
Materials Supervisor
SelfCharge Inc.

I received the 150+ boards yesterday afternoon. Thank you once again for your excellent service and quality. Be sure to thank the people in your factory for me as well. When I order from you, I know I don't have to worry about getting bad boards and going through the purchase cycle again. Let alone the embarrassment of explaining it all to my boss and his boss.

Warmest regards,

Richard Diehl
Maxim Integrated Products

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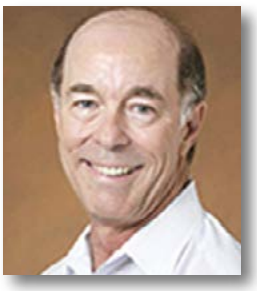
share his compelling vision of the design and technology innovations that will drive a new, very different future of personal transportation.

Day Three Keynote:
Thursday, February 21, 8:00-9:00 a.m.

B. Gentry Lee

Journey to Mars: Curiosity Rover Mission



On August 6, 2012, a mobile laboratory known as the Curiosity rover made an amazing landing on Mars. Curiosity boasts the biggest, most advanced payload of scientific instruments ever sent to the Martian surface. Its mission: to assess whether Earth's neighbor has ever had conditions favorable to life.

B. Gentry Lee, chief engineer for the Solar System Exploration Directorate at the Jet Propulsion Laboratory (JPL) in Pasadena, Calif., is responsible for the engineering integrity of the robotic planetary missions managed by JPL for NASA — including the wildly popular Curiosity rover mission. Join Lee for a fascinating inside look at the mission to Mars that has captured the imaginations of millions and learn about the feats of engineering that brought the Curiosity itself into existence.

IPC APEX EXPO Technical Conference

Tuesday-Thursday, February 19-21

The IPC APEX EXPO technical conference is known worldwide as one of the finest and most selective in the world. Learn about new research and innovations from key industry players in the areas of board fabrication and design and electronics assembly.

Sign up for one day, the full conference or get the most of your money with the Maximum Value Package. To register for the 2013 IPC APEX EXPO, click here.

Click here to search a complete listing of approximately 250 technical conference sessions by topic, category, speaker name, company, etc.

Education and Standards

The 2013 IPC APEX EXPO promises to deliver an impressive slate of educational programs and the largest technical conference for printed boards and electronics manufacturing in the world!

- Contribute to the discussions on the industry standards at more than 80 standards development meetings
- 52 half-day courses taught by experts will offer insights and strategies on the latest innovations and valuable tools
- International Academic Paper Competition — building stronger ties between academia and companies in electronics assembly, PCB manufacturing and design
- Certification programs will provide valuable credentials for EMS program managers and printed board designers
- The Designers Forum will focus on design education and networking with the option to add on an educational course in the afternoon

Professional Development Courses

February 17–18 and February 21, 2013

50 Professional Development course covering issues in design, lead-free technology, materials, process improvement, solder joint reliability and more will be offered at the 2013 IPC APEX EXPO. Going beyond theory, the courses will provide practical solutions to industry issues and challenges. Each course is led by a subject-matter expert, runs for three hours and will include an instruction handbook.

Industry experts such as Mike Carano of OMG, Happy Holden of Gentex, Cheryl Tulkoff of DfR, Bob Wetterman of BEST and Phil Zarrow of ITM will offer one or more courses. Course highlights include:

- Design for Manufacturing (DFM): Best Practices (PD08)
- Extreme HDI: Designing for Maximum Density (PD10)
- Best Practices in Electronics Assembly Processes (PD13 and 17)
- Tin Whiskers: Failure Risk and Mitigation Strategies (PD21)
- Ball Grid Array: Principle and Practice (PD30)
- Package on Package: Design, Assembly, Rework and Inspection (PD44)

"The courses at IPC APEX EXPO will enable engineering and management staff to work smarter in an era of increasing product sophistication," says Susan Filz, IPC director of industry programs. "Attendees will bring home new insights and solutions to boost their productivity."

Engineers like Rigo Garcia, Sr. Quality Assurance Engineer, NASA Goddard Space Flight Center agree, "The conference and courses offer a great opportunity to increase my value as a professional … and having the chance to talk to the technical experts and see equipment being used today is incredibly valuable."

Click here for a complete list of professional development courses along with full descriptions and instructor biographies.

Free IPC APEX EXPO BUZZ sessions

Seven free BUZZ sessions will be offered at IPC APEX EXPO this year. The industry's top technical experts on subjects ranging from automotive and new technologies to conflict minerals, export controls and technology roadmaps will provide insights into timely issues. Admission to the BUZZ sessions and the exhibit hall is free to pre-registrants, a savings of $25 on-site. For BUZZ session times and a complete schedule, click here.

Tuesday, February 19

Addressing "New Technologies," Jasbir Bath, IPC principal engineer for assembly technology, will lead off the BUZZ sessions. Bath will chair a discussion on new and emerging component technologies. Advancements in state-of-the-art electronic component interconnections will be one of the central themes. Then, C. Don Dupriest, Lockheed Martin Missiles & Fire Control, will moderate a panel featuring a "Who's who in electronics," during which IPC Hall of Fame Award recipients will take audience questions on technology and trends and share the wisdom earned from a collective 300-plus years of experience.

Wednesday, February 20

Chris Mitchell, Prime Policy, will moderate a panel on "Export Controls: Understanding ITAR and IT Reform." The panel of experts will provide

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Upcoming IPC Professional Development Events

February 19–21, 2013
IPC APEX EXPO® Conference & Exhibition
San Diego, CA

May 20–23, 2013
IPC ESTC™ — Electronic System Technologies Conference & Exhibition
Las Vegas, NV

June 4–5, 2013
IPC/FED Conference on Embedded Components
Frankfurt, Germany

June 11–13, 2013
IPC Conference on Flexible Circuits
Sponsored by Minco
Minneapolis, MN

August 20–22, 2013
IPC APEX India™
Bangalore, India

September 10–12, 2013
IPC Conference on Component Technology: Closing the Gap in the Chip to PCB Process
Sponsored by Amkor Technologies, Inc.
Chandler, AZ

November 12–14, 2013
IPC Conference on Solder and Reliability: Materials, Processes and Test
Costa Mesa, CA

More Information
www.ipc.org/events

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BUZZ sessions *continues*

an overview of International Traffic in Arms Regulations' (ITAR's) application to printed boards.

Later that morning, Fern Abrams, IPC director of government relations and environmental policy, will moderate a session on conflict minerals, which will provide an overview of conflict minerals disclosure and reporting regulation finalized by the U.S. Securities and Exchange Commission last August. A panel of experts will discuss tools for regulatory compliance and customers' requirements. And later that day, a session dedicated to "Automotive Technologies" will provide a current and future view of electronics technology used within the automotive electronics industry.

Thursday, February 21

The final two BUZZ sessions are on the reclassification of FR-4 composite materials and technology roadmaps. Crystal Vanderpan, UL LLC, will discuss UL initiatives and provide an update on UL recognition for laminate and printed board materials. In addition, Marc Carter, IPC director of technology transfer, will take session attendees on a tour of technology roadmapping efforts for printed circuit cards and electronics assemblies. He will highlight the major trends in the evolution of technology across multiple disciplines during the "IPC/iNEMI Technology Roadmap" session.

Designers Forum

Monday, February 18 • 7:30 a.m. – 1:30 p.m.

This program of education and networking is for all individuals with an interest in design. Designers Forum registration includes a networking boxed lunch following the program.

To view all design-related activities at IPC APEX EXPO, click here.

Designers Forum Agenda

7:30 a.m.	Check-in and Networking Breakfast
8:00 a.m.	Roadmapping for Design—Dieter Bergman, IPC Director of Technology Transfer
8:30 a.m.	Efficient Design Data Transfer to Manufacturing Using IPC-258—Edward Acheson, Principal Product Engineer, Cadence Design Systems Inc.
9:15 a.m.	Designing for High-Reliability Applications—Daniel DiTuro, Principal, DiTuro Consulting
10:00 a.m.	Break
10:15 a.m.	The Increasing Complexity of PCB Designs—Happy Holden, Director of Electronics Technologies, GENTEX Corporation
11:00 a.m.	Ask the Flexperts: Mark Finstad, Senior Applications Engineer, Flexible Circuit Technologies Mark Verbrugge, Program Manager, Pica Manufacturing Solutions
11:45 a.m.	Embedded Circuits: New Design Guidelines, Material Selection Variations, Termination Methodologies, Process Information—Vern Solberg, Consultant, Solberg Technical Consulting
12:15 p.m.	Professional Design: Technology and Technique—Rick Hartley, Sr. Principal Engineer, L-3 Avionics Systems
12:45 p.m.	Lunch
1:30 p.m.	Adjourn

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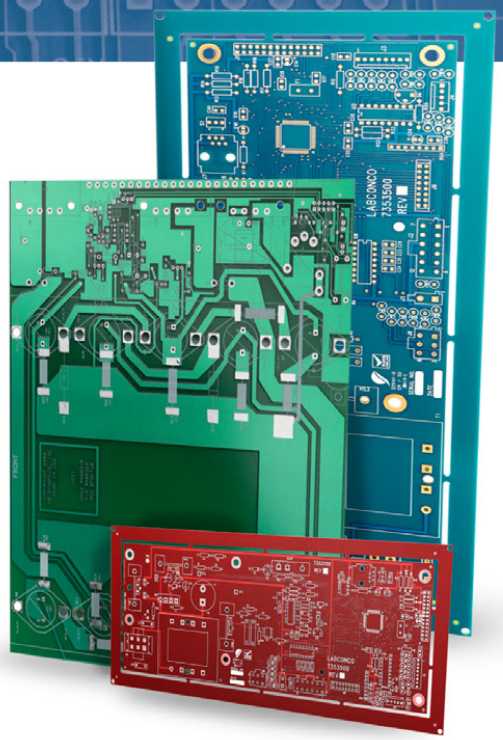

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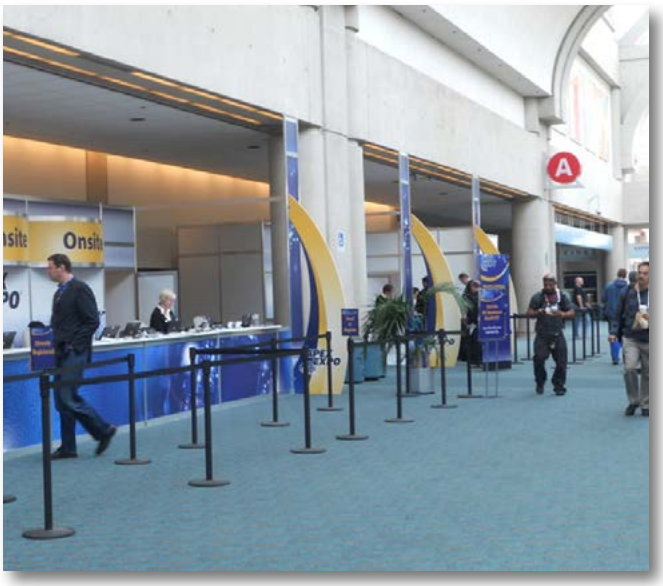
Programs for Executives

NEW! IPC PCB Supply Chain Leadership Meeting (View agenda)

Monday, February 18: 8:00 a.m. - 5:00 p.m.
Networking Breakfast: 7:30 - 8:00 a.m.
Networking Reception and Dinner: 6:00 - 9:00 p.m.



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  - Conductive Pastes
  - Embedded Components
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- Roundtable Discussions

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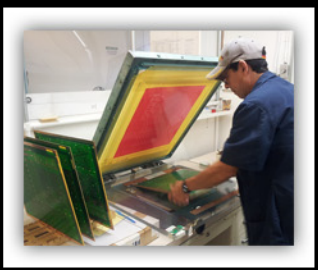
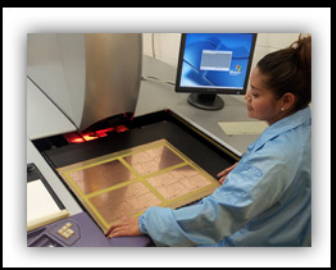

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High-Speed Boards Need Automated Checking

by Mike Steinberger
SISOFT

SUMMARY: A set of PCB prototypes typically costs $250,000 or more, not to mention a couple of months of schedule. The solution is to assemble all of the pieces of the system to see if they function correctly together, and it's faster and cheaper to do so in a simulation than it is to wait for hardware prototypes. Yet automated checking of high-speed serial channel interconnects at the board and system level is not common practice.

Progress

In 1984, at Bell Labs, I participated in the design of a 1,700-gate ASIC and a 2,300-gate ASIC intended to operate at the blazing clock rate of 150 MHz. These ASICs replaced a couple of boards full of ECL gate arrays, and were a major step forward in transmission system technology.

One of the emerging technologies we used at the time was a computer program that automatically checked the IC's manually generated layout before we went to mask. This replaced a process whereby engineers would plot the layout on paper, put the plot on the floor of a large room, and crawl over the plot with a pencil and schematic to verify that all the connections were correct. In those days, a mask set cost somewhere between $50,000 and $80,000 and a box of wafers cost $10,000; a mask re-spin cost a little over $100,000 and at least a month of schedule slip. That computer program prevented most re-spins and literally put money in my pocket.

Today, you can't even buy a site on an IC test shuttle for $100,000; automated layout checking programs have grown orders of magnitude more sophisticated, and such programs have long been an essential part of IC design.

Over the same time span, PCBs and systems have grown exponentially more complex as well. Many PCB designs today have many more nets than those ASICs I worked on back in 1984, and a fully populated card cage has at least an order of magnitude more nets than that. For any high-capacity system, most of those nets are for high-speed serial channels, and the design decisions required for those PCB nets are at least as complex as any of the ASIC design decisions we made in 1984. A set of PCB prototypes typically costs $250,000 or more and a couple months of schedule, so the same financial incentives are there as well.

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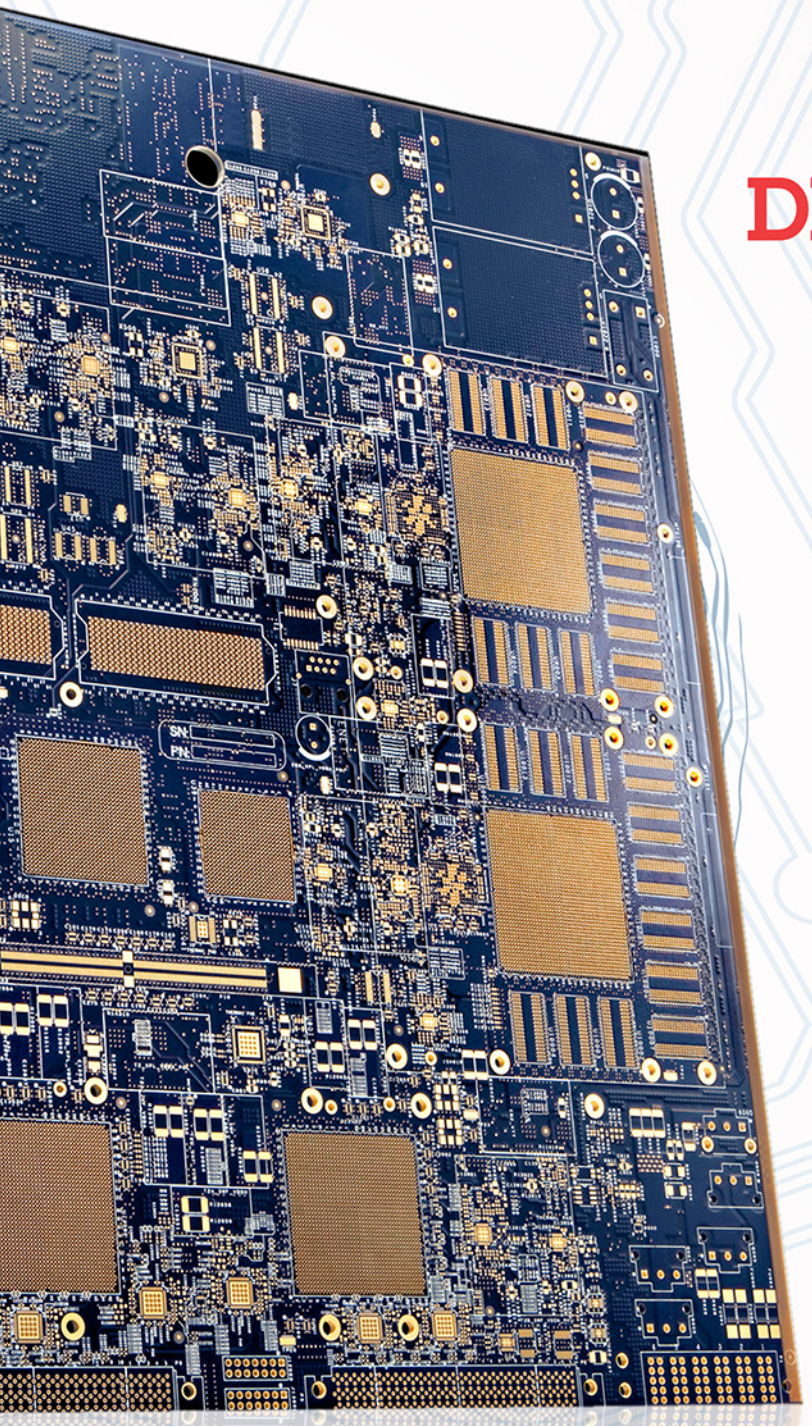

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And yet automated checking of high-speed serial channel interconnects at the board and system level is not common practice.

In a way, it is the complexity of the task that has impeded progress.

1. A system-level interconnect often involves multiple subassemblies such as plug-in cards, connectors, and backplanes. To check such an interconnect effectively, the descriptions of all of the subassemblies must be loaded into a single database for an end-to-end analysis.

2. The data rates are high enough and the physical structures are large enough that microwave analysis techniques are required to evaluate the behavior of the passive interconnect.

3. The drivers and receivers of these nets are sophisticated high-speed signal processing circuits containing equalization, clock recovery, and encoding/decoding. The behavior of these signal processing circuits absolutely must be included in the evaluation of the end-to-end performance.

4. The performance margins are so small that it is no longer practical to guarantee that every net has a positive timing margin that eliminates the possibility of bit errors. Rather, one must perform a more sophisticated analysis that predicts the probability of bit errors, and the goal of the design is to achieve a bit error rate that is below some very low target probability.

5. Even though the required analysis has a number of complex aspects, the turnaround time for the analysis must be short enough to be a part of an iterative circuit board and physical design process. Usually, many iterations of the design/analysis cycle will be required, and those iterations must be completed in time to meet a product development schedule. Ideally, board designers would like to get feedback overnight; but they seem to be able to live with a 48 hour turn-around time. Longer turn-around times are not acceptable.

This article describes a set of practical solutions to each of these challenges, as implemented in SiSoft's Quantum SI and Quantum Channel Designer products, and used to achieve first pass success in a complex data networking system that is now in production[1].

Post-Layout System Analysis

Since automatic PCB routing has been in use for a number of years, one would think that misconnections are a thing of the past. But for a complex system, that is definitely not the case. Even if the board designs were a perfect implementation of their schematics, there can still be detailed errors in the schematic's pin assignments. The problem can become even more severe when different PCBs are being designed by different groups or at different sites, possibly in very different parts of the world.

The solution is to assemble all of the pieces of the system to see if they function correctly together; and it's a lot faster and cheaper to do that in a simulation than it is to wait for hardware prototypes in a system lab.

Assembling a system for a simulation closely parallels the assembly of the real system:

- **Parts Procurement:** Circuit models are obtained for all of the parts that are to be included in the simulation. Usually, each model must be procured from the manufacturer.
- **Board Manufacture:** PCB layouts are processed to obtain a model of the interconnects provided by the bare board.
- **Board Assembly:** The circuit nodes of the parts models are associated with the circuit nodes of the PC board models.
- **System Configuration:** Usually, multiple boards are connected to complete the channels in the system interconnect. This requires that connector and pin numbers on each board are associated with connector models and then with connector and pin numbers on other boards. The system configuration also must include the configuration of the SerDes transmitters and receivers.
- **System Test Setup:** Operational parameters such as data rates, encoding, and channel impairments must be specified for the individual channels.

This is a lot of data in multiple formats to bring together from a lot of different sources. Assembling the simulations for a complex system is a major undertaking which is only possible if the simulation environment organizes the data and the tasks in a coherent way. The simulation

environment must also provide an organized way to modify the data, since the data is going to be updated and the simulations re-run every couple of days over a period of several months. Manual operations are unacceptable.

Post-layout simulation environments have been available for a number of years, and have matured to the point where it is practical to assemble system-level simulations for very complex systems.

Model Quality: When the analysis combines several different types of models and many models of each type, it is important to make sure that each model is suitable for the analysis to be performed. This task requires some engineering judgment, and so opportunities for automation are limited. It helps a great deal to work with vendors who provide documentation of the conditions under which their models are valid, and their models' correlation to measured or simulated data. These vendors are out there, but you have to find them.

Via Modeling

Given the data rates in current designs and the size of PCB structures, the PCB interconnect must be modeled as a microwave circuit. When this concept was introduced almost two decades ago, the focus was on the fact that signal traces needed to be modeled as transmission lines, and that reflections on transmission lines could have a substantial effect on the performance of both parallel and high-speed serial channels. By now, the transmission line models have become quite accurate over the entire frequency range of interest.

For perhaps the last decade, the primary challenge has been to model transmission discontinuities such as packages, connectors, AC coupling capacitors, and vias. Vias are a recurring theme in that they are used under packages and connectors, and as part of AC coupling structures.

Models used in the analysis of system level interconnects must satisfy two criteria:

1. The model must match measured data over the frequency range of interest.
2. The model must be produced quickly enough to satisfy the turnaround time requirements for the analysis flow.

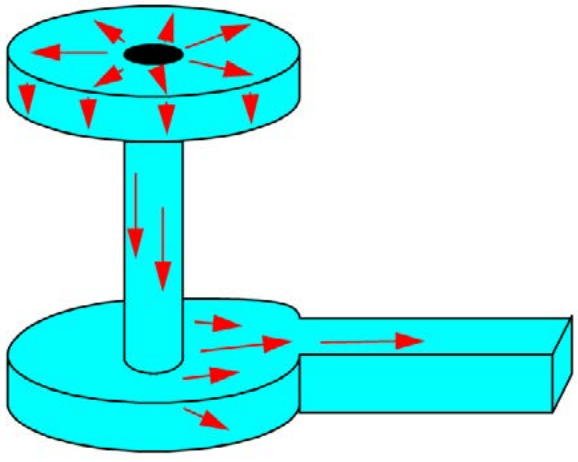

Figure 1: Via current flow.

For most of this decade, mesh-based 3D electromagnetic field solvers have been the primary tool used to study vias. Field solver analyses of even a single via design take hours to run. A single PCB design will typically have many different via configurations, and those configurations can evolve with each iteration of the board design; so regardless whether they satisfy the first of the requirements above, field solvers clearly do not satisfy the second requirement.

More recently, several papers[2, 3, 4] have demonstrated good correlation to measured data for a model which represents the via as a short length of transmission line. This work has been extended[1, 5] to demonstrate that even better correlation to measured data can be obtained by adding to the via model an equivalent circuit for the pads and exit traces at the top and bottom of the via.

Figure 1 illustrates that the via model should follow the path the current actually takes along the surface of every element of the via structure including the top pad, via barrel, bottom pad and exit trace.

Figure 2 and Figure 3 are typical examples of the correlation between model and measured data that can be achieved using this type of model. Figure 2 is a time-domain reflectometry (TDR) result demonstrating that the model does a good job of matching the impedance vs. physical location at each end of the channel while Figure 3 demonstrates the degree to which the

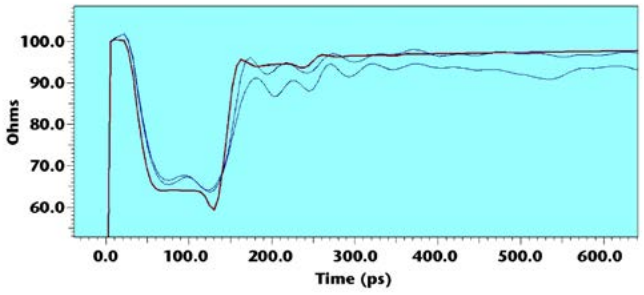

Figure 2: Typical differential TDR correlation result.

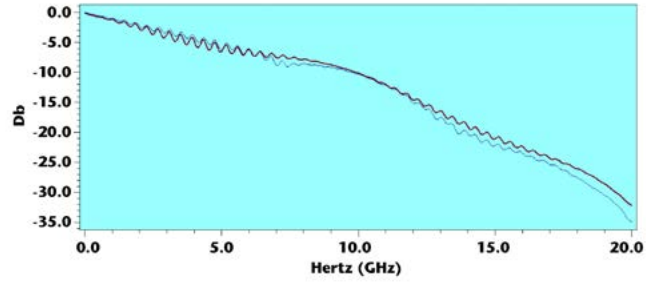

Figure 3: Typical differential insertion loss correlation result.

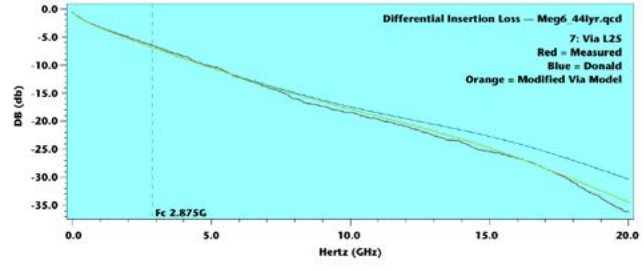

Figure 4: Modeled vs. measured insertion loss with empirical via loss model.

insertion loss predicted by the model matches measured data.

The effort to improve the match between model and measured data has continued. Some of the latest results[6] suggest that at higher frequencies, substantial losses occur at the vias themselves. As data rates get above about 10 Gb/s, these losses should be included in the via models.

Figure 4 shows one of the results from[6] using an empirical loss model. The measured data is shown in red and the result using a model from the same generation as that which produced Figure 3 is shown in blue. The result from the latest empirical via loss model is shown in gold.

All of the models described by[2, 3, 4, 6] are generated from equations that can be evaluated in a fraction of a second. Thus, these models both match measured data and can be produced so quickly that they do not affect system analysis turn-around time.

IBIS-AMI Modeling

The IBIS-AMI (Algorithmic Modeling Interface) standard[7, 8, 9] was developed to provide an efficient way to model the sophisticated processing that can occur in the transmitters and receivers (SerDes macros) associated with a high-speed serial channel. These models are delivered in a compiled, executable form that complies with a standardized software interface. Because it is supplied in compiled form, an IBIS-AMI model has several desirable characteristics:

- Since it is written using a general purpose programming language, the model can implement whatever behaviors the model developer chooses.
- The model can execute very quickly. For most models, a million-bit time-domain simulation only takes a few minutes.
- Models from different IP vendors can be combined in a single analysis or simulation. For example, the transmitter from one vendor can drive the receiver from another vendor.
- The models are portable between EDA tools.
- It is impractical to reverse engineer the model, so the model protects information that is proprietary to the IP vendor.

Because of these characteristics, it is practical to include IBIS-AMI models in a system-level analysis or simulation, and IBIS-AMI modeling is one of the technologies that en-ables the end to end analysis of high-speed serial channels.

Model Quality: The IBIS-AMI standard has been in place for over four years, and most ven-

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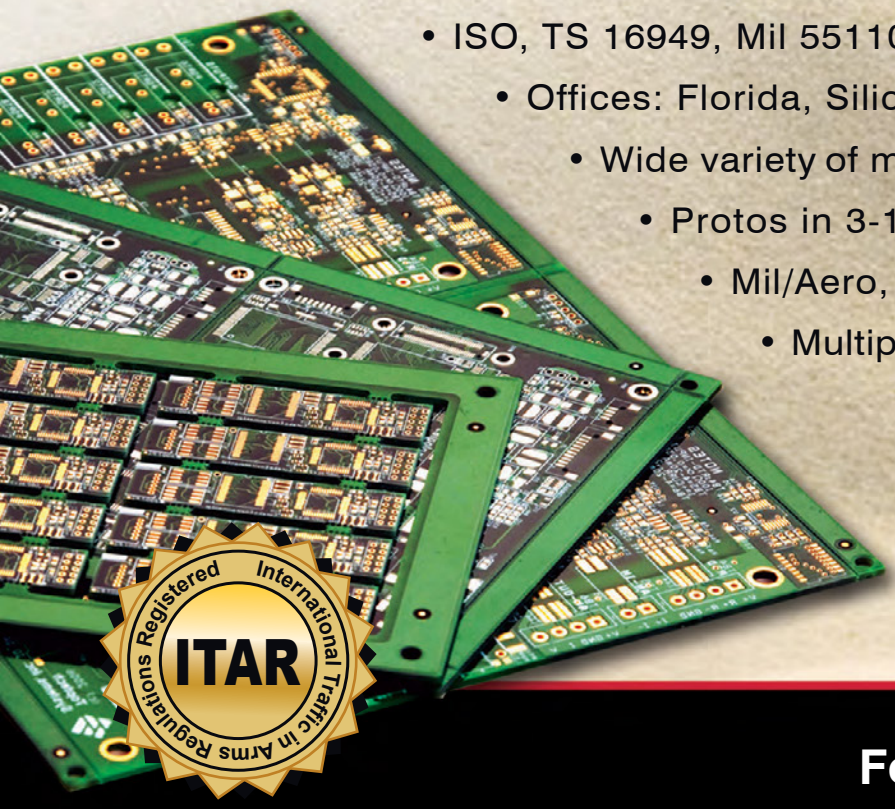

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dors now supply IBIS-AMI models of the SerDes macros. Some of these models are excellent – fast, accurate, flexible, and correlated to measured data while others have serious deficiencies that need to be understood in order to obtain valid results. This is one area where the user should be particularly careful to make sure they understand the capabilities and limitations of the models they're using. Some vendors supply documentation which makes this task a lot easier.

Performance Analysis

There are two generic approaches to bit error rate estimation: statistical analysis[10] and time domain simulation.

For time domain simulation, a time domain waveform is generated and then analyzed to predict the bit error rate. Time domain simulations of high-speed serial channels typically need to be run for a million bits or more to get a reasonable sample of the channel distortion and equalization. They therefore take several minutes each to run in order to produce meaningful results. While this isn't a serious problem when there are only a few simulations to run, the time required becomes unacceptable when there are a few thousand simulations to run.

The other option, statistical analysis, typically runs in a few seconds, but has its own limitations. Statistical analysis calculates the statistics of the signal directly rather than accumulate them through samples of the signal. In order for this technique to be rigorously applicable, however, the signal must be the result of a linear, time-invariant process. Thus, amplifier saturation or the time-varying behavior of control loops forces statistical analysis to become an approximation rather than a precise calculation. Depending on the AMI models used, however, this approximation can be more than accurate enough to drive reliable engineering decisions.

AMI models have two modes of operation: statistical analysis and time domain simulation; there are no guarantees that the two modes will produce identical results. The statistical analysis mode of the model often requires more insight and creativity from the model developer and specialized numerical processing techniques in the model. This is especially the case for models of nonlinear receivers. Nonetheless, there are many models of nonlinear receivers in widespread use that provide consistent and accurate results in both statistical analysis and time domain simulation.

Model Quality: Automated checking at the system level requires AMI models that produce accurate results in statistical analysis mode.

Data Mining

Using the technologies described above, it is practical to automatically analyze thousands of nets, thus producing tens of thousands of data files. Automated methods are required to turn all that data into information.

The first question is whether or not all of the nets are connected correctly. For nets that connect a transmitter on one plug-in to a receiver on another plug-in across a backplane, one very effective method is to compare the total length of the net to the length of the backplane trace used. A typical result is shown in Figure 5.

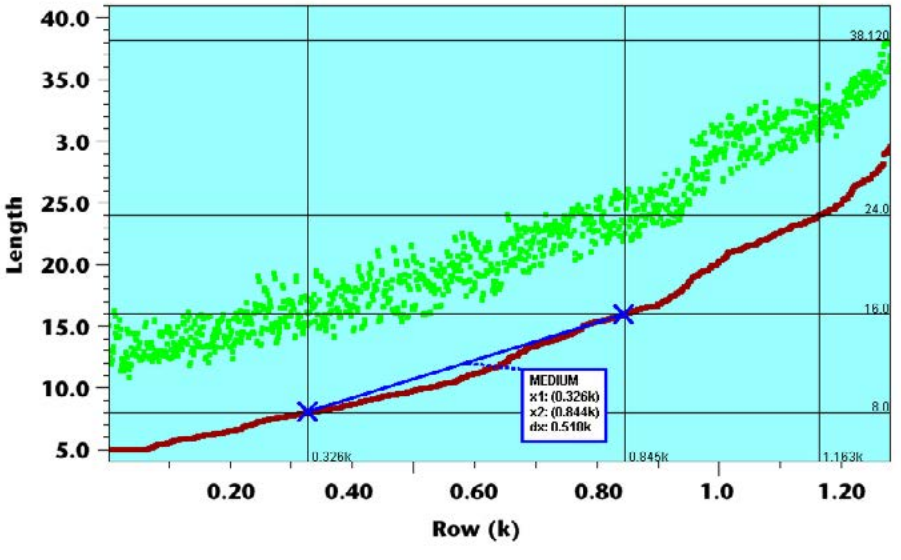


Figure 5: Physical connectivity: backplane and total net lengths.

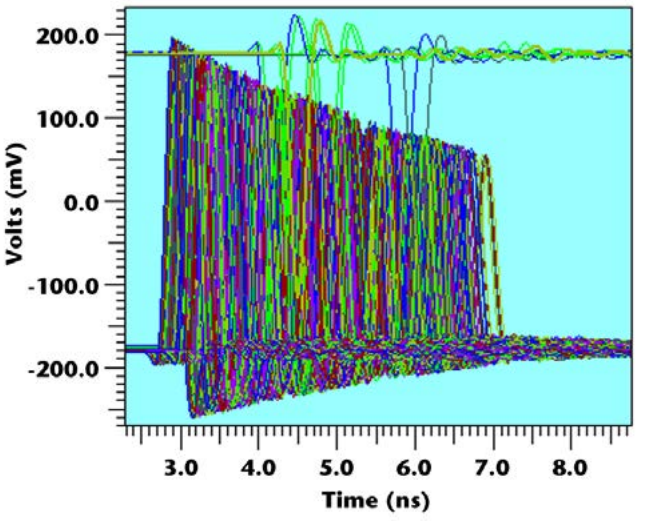


Figure 6: Operational connectivity: pulse responses.

In Figure 5, each net populates a separate column of the graph. In this case there are 1,280 of them. The backplane length is shown in red while the total length is shown in green. The nets have been sorted by backplane length. In this particular example, each green dot is significantly higher than the corresponding red dot, indicating that all of the nets are connected.

It is also relatively easy to identify nets which have had their polarity reversed ("swizzled"), with the P-pin of the transmitter connected to the N-pin of the receiver, and vice versa. Figure 6 is a plot of the pulse responses for all of the nets analyzed. In addition to illustrating the range of delays and insertion losses in the system, this figure shows that there are a few nets that have been swizzled, in that they transition from high to low rather than low to high. In the waveform viewer, the swizzled nets can be identified by clicking on their pulse response.

The next quick check is to make sure that all of the high-speed serial channels have positive timing margin (eye width) and amplitude margin (eye height). Figure 7 is a scatter plot of eye width and eye height for each net, with the nets sorted in order of decreasing eye height. While most of the nets in this example have positive margin, there are two that don't, as is evident through close examination of the right hand side of Figure 7.

It is not at all uncommon to have a couple of nets with no margin in an otherwise healthy system. Furthermore, the nets that have a problem are seldom the longest nets[11, 12]. One of the most common problems is that a relatively short net has some relatively large discontinuities in it, resulting in resonances that can be hard to equalize. These resonances are a very sensitive function of materials properties, and a slight change in dielectric constant will move the problem from one set of nets to another. When this happens, it's best to identify an entire class of nets that have similar lengths between similar discontinuities, and to fix all of them by somehow reducing the discontinuities. The procedure will depend very much on the system and the nature of the discontinuities; however, data mining procedures similar to the examples above can often help to identify the nets that need to be fixed.

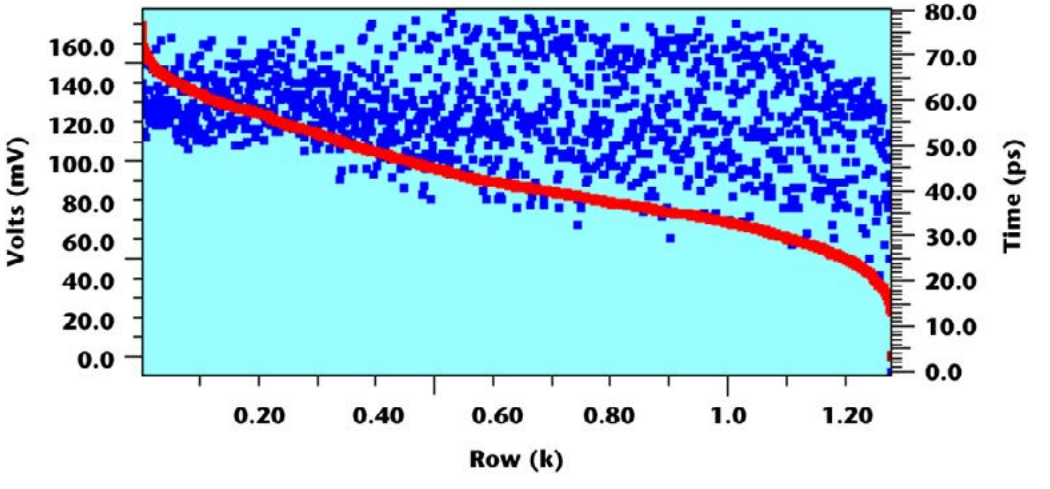
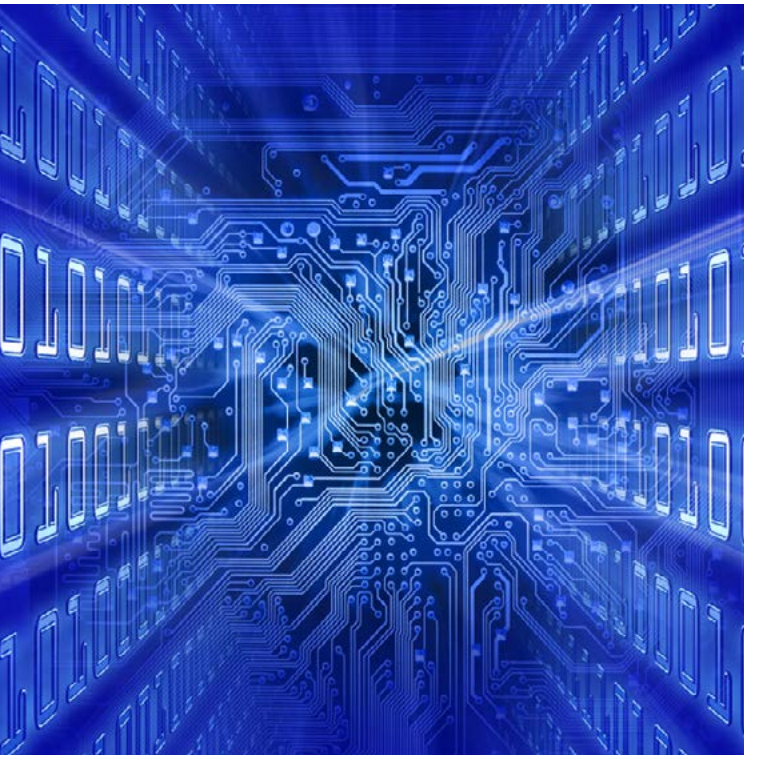


Figure 7: Operational connectivity: 10-12 eye heights and widths.



Reference 1 describes many other ways in which the data from automated checking can be mined to provide useful information.

Conclusion

All of the technologies needed to make the automated checking of high-speed boards practical are now available, and have been integrated and used on systems that are now in production. This automated checking has made first pass success a reality for system development in the same way that automated checking of IC layouts brought first pass success to IC designs.

The simulation results generated by the automated checking process can also be used to identify ways to improve the system's performance margin, and to optimize the system configuration on a per-link basis. This is an interesting topic in its own right. **PCBDESIGN**

References

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Dr. Michael Steinberger, lead architect at SiSoft Inc., is responsible for the architecture of SiSoft's Quantum Channel Designer tool for high-speed serial channel analysis. He has more than 30 years of experience in the design and analysis of very high-speed electronic circuits. Before joining SiSoft, Steinberger led a group at Cray Inc., performing SerDes design, high-speed channel analysis, PCB design, and custom RAM design. He holds 14 patents.

Most-Read Mil/Aero007 News Highlights

All Flex Acquires Part of TRI-C Design

The acquisition of TRI-C Design's assets and design services adds five people to the expanding company consisting of 140 employees between the Northfield facilities and a third production facility in Bloomington, Minnesota.

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Ventec Europe Managing Director Mark Goodwin said, "This accreditation confirms our emerging position as a leader in the design and manufacture of high-reliability materials for the military and commercial aerospace sector. I believe Ventec International Group is the only copper clad laminate and pre-preg manufacturer with this accreditation."

U.S. Military: $909.3M Budget in Vetronics Procurement

New analysis from Frost & Sullivan, U.S. Military Vetronics, finds that the 2013 U.S. military budget requests $909.3 million in vetronics procurement, which will decline at a rate of 8.6% until 2017.

Global Homeland Security Market to Reach $281B by 2022

In a report titled "The Global Homeland Security Market 2012-2022 - Market Size and Drivers: Market Profile," market analyst Strategic Defence Intelligence forecasts that the global homeland security market will reach $198 billion in 2012 and increase at a CAGR of 3.55% during the forecast period to reach its peak of $281 billion by 2022.

Report Examines UK Defense Industry Through 2017

"Industry Market Opportunities and Entry Strategies, Analyses and Forecasts to 2017" offers the reader an insight into the market opportunities and entry strategies adopted by foreign OEMs to gain market share in the UK defense industry.

N.A. Military Avionics Market Report 2012

As pressure on the budgets of both countries forces reassessments of that spending, the military services will need to think strategically about the future procurements and methodologies.

Commercial Aircraft Cabin Lighting Market at $1.25B by 2017

According to a new market research report, Global Commercial Aviation Aircraft Cabin Lighting Market, Forecast & Analysis (2012 - 2017), the total global commercial aviation aircraft lighting market is expected to reach $1.25 billion by 2017 with a CAGR of 5.43%.

Global UAV Payload Market to Hit $68.8B by 2022

With the expected growth in market demand and diversity in UAV applications, there is a growing requirement for the future UAV and payload design to combine multi-mission, modular, open architecture features, capable of accomplishing diverse missions.

Nanowires Could Lead to More Efficient, Cheaper Solar Cells

In the latest issue of Science, researchers from Lund University in Sweden have shown how nanowires could pave the way for more efficient and cheaper solar cells.

"Our findings are the first to show that it really is possible to use nanowires to manufacture solar cells," says Magnus Borgström, a researcher in semiconductor physics and the principal author.

The nanowires are made of the semiconductor material indium phosphide and work like antennae that absorb sunlight and generate power. The nanowires are assembled on surfaces of one square millimeter that each house four million nanowires. A nanowire solar cell can produce an effect per active surface unit several times greater than today's silicon cells.

Do Not Measure PDN Noise Across Capacitors!

by Istvan Novak
ORACLE

SUMMARY: There are a variety of ways to measure PDN noise, but measuring across a capacitor will attenuate the high-frequency burst noise. Keep in mind that by measuring across a capacitor, the converter output ripple reading could be several times higher – or many times smaller – than the actual ripple across our loads.

Some application notes will tell you that to measure the output ripple of a DC-DC converter, the best way to make the connection is to attach the probe across the top of one of the output capacitors. While there is a legitimate argument for measuring the noise this way, be aware: if you measure the noise across a capacitor, it will most likely alter the noise signature.

Take, for instance, the evaluation board shown in Figure 1. It holds a small, encapsulated step-down, non-isolated DC-DC converter – the black rectangular package in the middle of the board. I use this board in my courses to show live measurements of converter loop stability and output impedance. This is very convenient for desktop demos, because the input voltage range is a few volts, so the entire setup can be powered simply with three AA batteries. The converter can be loaded with up to 4A of current. In addition to the converter module, which contains a fully functioning DC-DC converter[1], the evaluation module has banana receptacles for connecting the input supply and the load, a few ceramic capacitors across the input and output terminals, jumpers for setting the output voltage, and two BNC receptacles to connect oscilloscopes.

There are spare footprints for experimenting with additional components: CO4 is a capacitor footprint across the output terminals. It is marked by the white arrow and label in the top view of Figure 1. There is also a populated site with a 100uF ceramic capacitor at that same exact location (CO5), on the back side of the board. The DC load can be connected with banana plugs to the receptacles above and below of these capacitors.

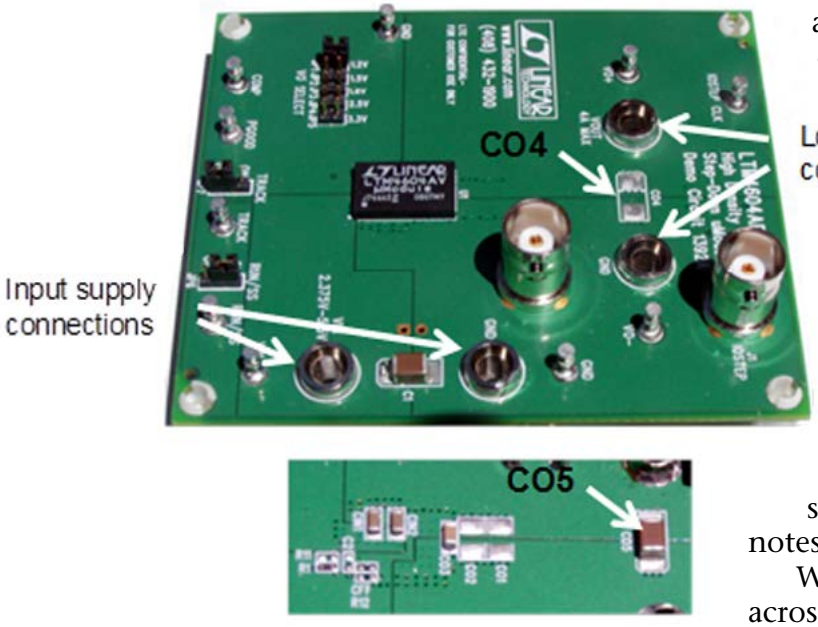

Figure 1: Top view (top) and partial bottom view (bottom) of the evaluation board for a Linear Technology LTM4604 DC-DC converter. Evaluation module courtesy of Linear Technology.

We can take an oscilloscope[2] and a homemade semi-rigid probe and measure the output ripple of the running converter at different locations. Figure 2 shows the connection of the probe across the top side of CO5, similar to how application notes may suggest.

We can also connect the same probe across the vacant capacitor site, CO4. Remember, these sites are at the same location on the board; CO4 on the top, CO5 on the bottom. Since we measure the output ripple at the same location on the board, we would

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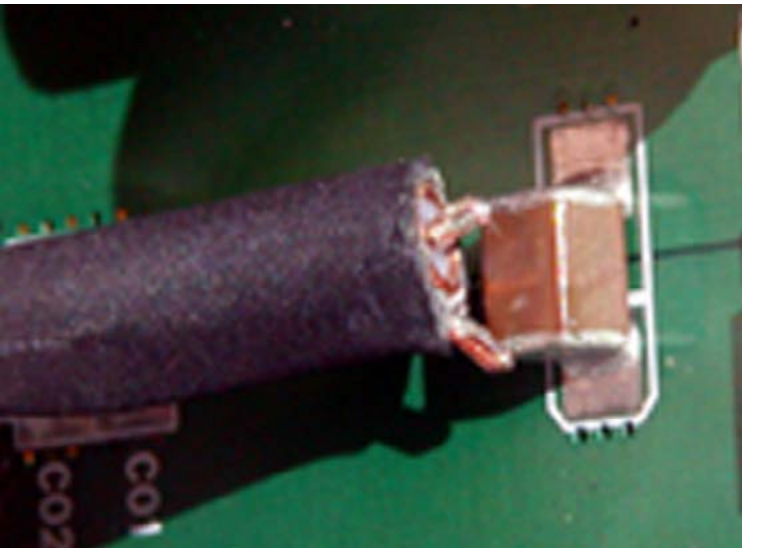

Figure 2: Connecting a homemade semi-rigid probe across the top terminal points of an output capacitor, CO5.

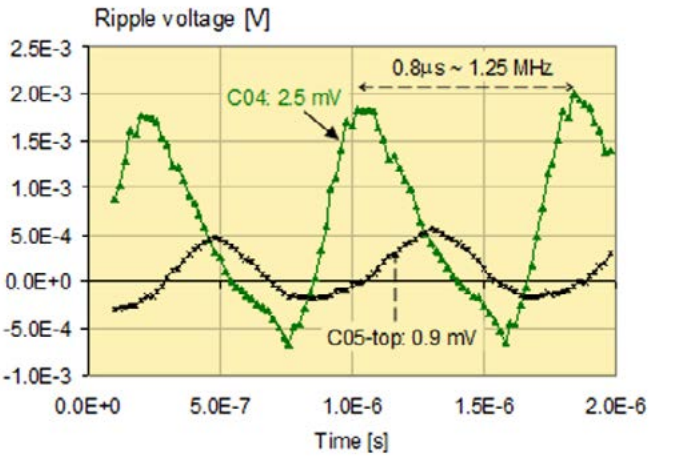

Figure 3: Output ripple waveform of the running DC-DC converter module, measured at the same location on the top (CO4) and on the bottom (CO5, across the capacitor terminals). The magnitude ratio at the two locations is approximately 3x.

expect to see the same voltage. This is not the case, however, as it is shown in Figure 3.

We can see that the voltage waveform across the top terminal points of CO5 is almost sinusoidal and the magnitude is 0.9 mVpp. When we measure across the vacant capacitor site on the other side of the board, we get a more distorted, harmonic-rich waveform, and almost three times bigger magnitude: 2.5 mVpp. Why do we have such a big difference, when we measure practically at the same location? We can find the answer by looking at the equivalent circuit of our connections. Figure 4 shows the equivalent circuit when we measure across the top terminals of a capacitor, CO5 in our case.

The bottom of the equivalent circuit connects to the power and ground planes. This is where we really want to know the output ripple. Why on the planes (which are usually inside the PCB stackup) and not on the surface, across a capacitor? Because the loads this converter has to feed are connected to the converter through the planes. The planes will carry any output ripple from the converter output to the load. We don't have any load connected across the top terminals of capacitors, and therefore the voltage there is irrelevant for our purposes. Instead, we need to know the noise across the planes.

No matter how carefully we attach our measuring probe, we will always have some parasitic impedance in the path. In Figure 4, the parasitic impedances are represented by four components in each leg: a resistance and inductance representing the series impedance of through-holes or vias connecting between the planes inside the board stackup and the surface, and a resistance and inductance representing the series impedance of surface pads. These series impedances are usually small compared to the input impedance of our measuring instrument. We are talking about milliohms and nanohenries. These series impedances would create no significant distortion in the measurement results if we had no shunt element across our measuring instrument.

But when we measure across a capacitor, we have the equivalent series C-R-L circuit of the capacitor across our measuring instrument. And because bypass capacitors are supposed to have low impedance, this shunt leg in the equivalent circuit will form a frequency-dependent voltage divider with the series impedances of vias and/or pads. We can easily calculate the transfer function of our measurement connection.

DO NOT MEASURE PDN NOISE ACROSS CAPACITORS! *continues*

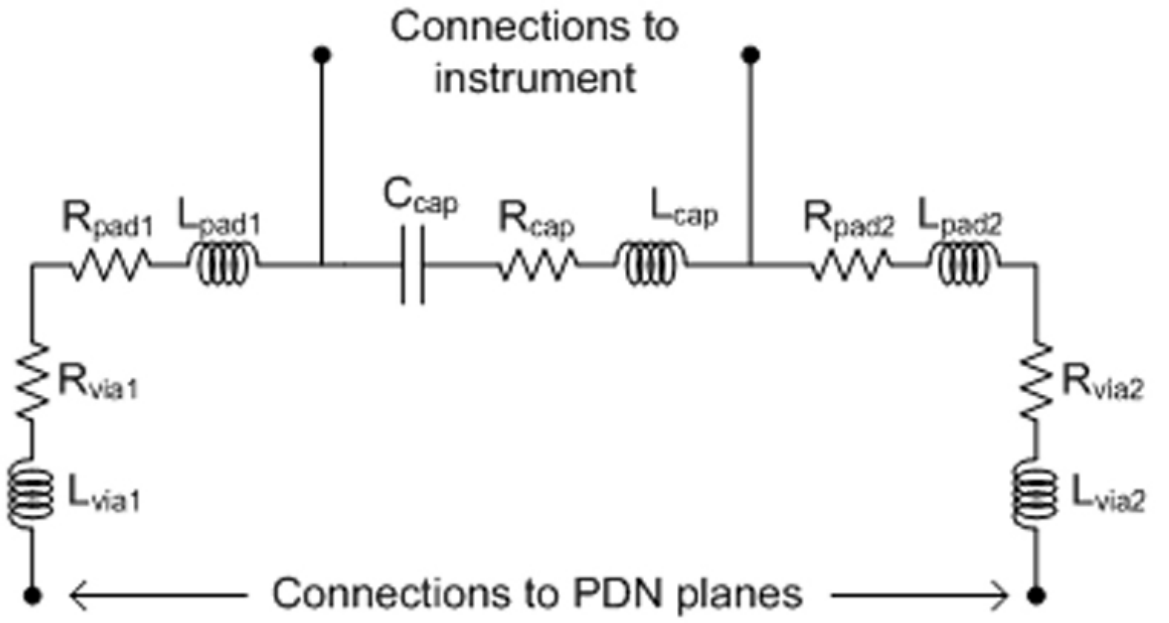

Figure 4: Equivalent circuit of the connection when measuring across a capacitor.

We can do it either in a spreadsheet, coding the transfer function, or using circuit simulators to get the answer.

With typical values, such as a milliohm of via and pad resistance and a couple of nH via/pad inductance, we get a transfer function shown in Figure 5. At low frequencies we get no attenuation and no gain, because the shunt impedance of the capacitor is high. As the frequency increases, the impedance of the capacitor drops inversely with frequency and we go through series and parallel resonance frequencies. These resonances create a peak (gain) and a dip (high attenuation), followed by the high-frequency asymptote, which is set by the ratio of inductances of the capacitor and vias/pads.

The equivalent circuit of Figure 4 is generic, and it can be also be used for cases when we have power planes only inside the stackup and not on the surface. The evaluation module we use here has multiple plane layers in the stackup and there are power and ground patches both on the top and bottom layers.

Note that the vertical scale of Figure 5 is logarithmic; we can have a large ratio between the peak and dip of this transfer function. With our example numbers, this ratio is approximately 30. We get 3x amplification at the resonance peak and a 10x attenuation at the resonance dip. The high-frequency attenuation is approximately 3x. By comparing with data from Figure 3, we see that we get approximately 3x attenuation of the switching ripple when we measure across a capacitor.

So, why would someone measure the converter output ripple across a capacitor? There

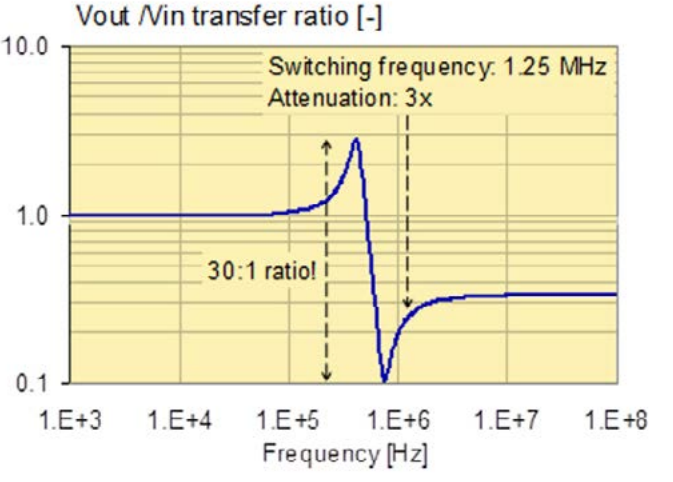

Figure 5: Typical transfer function of the measurement connection when we measure across the top terminal points of a capacitor.

DO NOT MEASURE PDN NOISE ACROSS CAPACITORS! *continues*

is a lazy answer and there is also a legitimate reason. The lazy answer is that there may be circuits where there are no dedicated test points or vacant component sites where we could conveniently probe the noise and ceramic capacitors having exposed side metallization extending all the way to the top of the part offer convenient connection points. The legitimate reason could be that DC-DC converters create not only the switching ripple as output noise, but also high-frequency burst noise. Measuring across a capacitor will attenuate the high-frequency burst noise. But whether we are just lazy or want to attenuate the high-frequency burst noise, we have to keep in mind that by measuring across a capacitor, the converter output ripple reading could be several times higher or many times smaller than the actual ripple across our loads.

You can read more about DC-DC converter characterization and measurements in *Dynamic Characterization of DC-DC Converters*[3]. **PCBDESIGN**

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Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. Novak received his M.S. degree from the Technical University of Budapest, Hungary and his Ph.D. degree from the Hungarian Academy of Sciences in 1976 and 1989, respectively. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To contact Istvan, click here.

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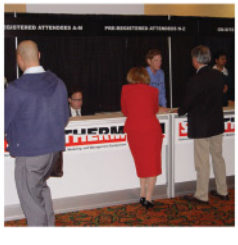

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Is the Cloud a New Paradigm for Electronic Design?

by Dr. Raul Camposano and Steven McKinney
NIMBIC INC.

SUMMARY: *There's a buzz surrounding the cloud, and how computing is moving to it. Most know that a cloud is a remote storage location to back up files, but is it more than that? What is the cloud in the context of computing, and what are the benefits for PCB design companies?*

A cloud is typically defined as a set of virtualized resources, most commonly software, platforms, and infrastructure that can be accessed through the Internet. Cloud computing can be private, meaning that the resources are in-house, or they can be public, where a company offers cloud infrastructure as a service. To be useful, clouds tend to be large, providing the illusion of unlimited resources and are often associated with service (as opposed to licenses or capital goods) as a business model. One example is software as a service (SaaS).

A commonly held view is that the cloud is shifting the computing paradigm: Simply put, large-scale commodity computing (millions of servers) virtualized and delivered through the Internet is better than smaller compute centers, regarding cost of ownership, scalability, performance, and utilization. As a result, the cloud is being adopted widely across consumer and enterprise applications. We use cloud-based applications every day with e-mail, search, social media, and gaming. Every time you pick up your smartphone, the apps rely on sourcing data from another location over the Internet, which is cloud-based. Indeed, the cloud plays a role in our daily lives, but how can it be beneficial to electronic design?

At first glance the advantages of the cloud for designing integrated circuits, packages, and boards may seem obvious:

- Numerous parallel jobs running simultaneously.
- On-demand computing resources.
- No need to purchase computers or tools upfront.
- Eliminates the need for dedicated IT staff.

But despite these benefits, electronic design has been a laggard in adoption of the cloud. As the first EDA company to have the cloud as a core component of its DNA, Nimbic often hears the concerns of organizations and their reasons for not adopting the cloud, so let's take a look at some of these and put them to the test.

1. Security

This is often the initial concern with using a public cloud. However, every day, millions of people entrust the Internet with some of their most important banking and financial data with little concern, so it seems reasonable that electronic design data can be handled in the same manner. Transmitting data through

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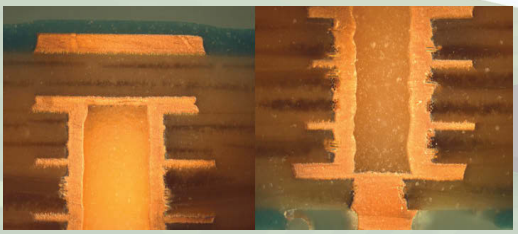

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the Internet can generally be as secure as your own network through use of security protocols, encryption, and authentication. However, there are other components to security: auditability and accountability. Once the data has reached a public cloud, there is no real way of auditing or verifying the accountability of the service provider to secure your data because processing data in a "secure" manner is harder than transmitting data securely. We address this issue with dedicated personal nodes (p-nodes) for each user and personalized encryption keys for data transmission, ensuring that you have the most secure environment possible.

2. Large Data Files

A design flow consists of many tools, even several dozen different tools for a complex application, and these tools often read and write large data files. Unless all the tools in the design flow are available in the same cloud, these files need to be transferred through the Internet. Transferring a terabyte through a (fast) 100 megabit/second Internet connection takes about one day and costs approximately $100 (the typical 2012 cloud price). Integrated circuit design generates terabytes of data at some stages, so this starts to get expensive in both time and hardware costs. However, package and PCB designs generally are smaller amounts of data, making it practical to transmit these through the Internet. So while a complete design flow from IC to board may not be practical, our solution focuses on fragmenting what is done in the cloud.

"Many design applications involve interactive graphics and network latency, making it challenging to run such applications remotely."

3. Interactive Graphics

Many design applications involve interactive graphics and network latency, making it challenging to run such applications remotely. To ensure instantaneous response of an interactive application, the round-trip time between the client and the cloud providing the computing must be in the tens of milliseconds at most. The theoretical limit for fiber is about 16 ms for 2,000 miles round-trip; in practice, latency is much higher, depending on the number of hops and the distance to an Internet backbone, among other things. Interactive graphics in the cloud is only possible using modern technologies such as WebGL, which load a model of the graphics being displayed locally and execute graphic operations locally. The alternative is to have local installations of the graphical interface and all heavy processing happens in the cloud to utilize the performance and demand elasticity offered in the cloud.

4. Existing In-house IT Resources

Companies involved in electronic design typically have extensive in-house IT resources, including an IT department and policies. They deploy design software, which they either buy or lease long-term, typically 1-3 years. Overcoming this way of doing things is perhaps the largest logistical obstacle to adopting the cloud. It also blurs the real cost of deploying design software in-house, since these resources already exist and the incremental cost of deploying one more application is low and hard to quantify. In cases where no in-house IT resource exists and IT is handled through contracting, the cost/benefit analysis is easier to understand and quantify.

5. Cost

One of the key promises of the cloud is cost reduction. There is little doubt that eventually the cost of using computing power generated by large utility-type data centers with millions of servers will be lower than the cost of deploying your own small- to medium-size computer center. However, at present this is still not the case. For example, consider infrastructure as a service. Today, a typical, fast 8-core machine with 64 Gb of memory costs on the order of $1 per hour in the cloud, which comes to $8,760 per year if used 24 hours a day, 7 days a week. Such a server would cost on the order of $3,000, or $1,000 per year if depreciated in three years. Hosting it (rack, power, AC, Internet) costs about another $1,000 per year, making the hardware-

only cost $2,000 per year (purposefully neglecting other costs such as maintenance, personnel to run a data center, etc.).

So, from a hardware point of view, if the machines are used more than 2000/8760 ~ 20% of the time, buying is cheaper than using the cloud. There are, of course, different calculations, but the point is that cloud computing is not clearly cheaper, unless the average utilization of the resources is low. The utilization of design software licenses that cost hundreds of thousands of dollars is likely to be high, so running it locally is often still more cost-efficient than running it in the cloud.

"The cost of the computing resources should be small compared to the cost of the software, which is the case for most integrated circuit design solutions."

6. Business Model

The argument for SaaS – or pay-per-use – is similar to the cost argument above. If the utilization of the software is low enough, SaaS is more cost-effective. However, most companies are used to and prefer a more predictable licensing or a 1-3 year subscription model. As already pointed out, expensive software tends to have a high utilization. Users also may receive considerable discounts when they purchase design software in large volume, which offsets the attraction of the SaaS model for the electronic design space.

So, what does work? Which electronic design applications are expected first migrate to the cloud first? For an application to work well in the cloud, it must not exhibit the 6 issues listed above, and must meet the following characteristics:

1. Security requirements are not extreme; a PCB or a package is a better design candidate for the cloud than the latest and greatest microprocessor or an ITAR (International Traffic in Arms Regulations) design.

2. Transmit small amounts of data compared to the computation time; the data transmission time needs to be almost negligible in comparison to the time the application will run. The data associated with early design stages (e.g., netlists as opposed to layouts) and with packages and PCBs is typically small enough to be transmitted quickly through the Internet.

3. No interactive graphic user interface, or the graphics should be separated from the computation and run locally. For example, a schematic editor can be run locally and the data for the simulation of the resulting circuit can be sent to the cloud, which may require extensive compute resources not available locally.

4. The organization would likely have limited in-house IT resources or have an IT department that is actively moving applications to the cloud.

5. The cost of the computing resources should be small compared to the cost of the software, which is the case for most integrated circuit design solutions. Or the utilization of the application should be low enough on average to benefit from temporarily allocated cloud resources. A third case arises if a design application can leverage parallelism and temporarily run multiple copies of the software across many machines to accelerate a task: 1 computer for n hours costs the same as n computers for 1 hour. Exploiting this elasticity is one of the core value propositions of the cloud. In the case of electronic design, this elasticity can be extremely beneficial in reaching a short time to results for compute tasks that may normally take hours or days, such as electromagnetic simulation. In a compressed engineering schedule, this can mean the difference between making or missing your market window.

6. Providers of design software in the cloud need to offer predictable subscription business models to satisfy average loads in addition to pay-per-use for peak loads.

Many applications in the design of electronic systems are starting to move or are ready to move to the cloud. To name a few:

- Electromagnetic simulation.
- Design and manufacturability rule check for PCB and packages (in most cases the

IS THE CLOUD A NEW PARADIGM FOR ELECTRONIC DESIGN? *continues*

Internet is still too slow to transmit chip layouts in a reasonable time).
- Library characterization.
- Variability analysis for cells, analog circuits, packages and boards.
- Functional, logic and circuit simulation.

As the cloud matures, all but a few applications (e.g., applications with extreme security requirements), will move to the cloud. It will naturally be adopted first by the users who benefit most right away, such as small companies with limited or no IT resources. It is also more likely that designers of printed PCBs and packages will be earlier adopters than IC designers due to the design size. Price and convenience are the ultimate differentiators, and large scale "utility" public clouds will at some point be cheaper than any alternatives, offering virtually unlimited resources on demand. Migration of electronic design to the cloud will happen, but the speed of migration will depend on the successes, failures, and costs along the way. **PCBDESIGN**

Dr. Raul Camposano has over 25 years of experience in electronics and design technology with careers in industry and academia. He is currently the CEO of Nimbic, a startup developing design technology for electromagnetic simulation in the cloud. Formerly the CTO of Synopsys, Raul was elected Fellow of the IEEE in 1999.

Steve McKinney is an application engineer at Nimbic, where he helps package and PCB design engineers address their high-speed modeling challenges with Nimbic's electromagnetic tools. He has over 10 years of experience working in high-speed signal/power integrity design and simulation tools. Steve has a BSEE and MSEE from North Carolina State University.

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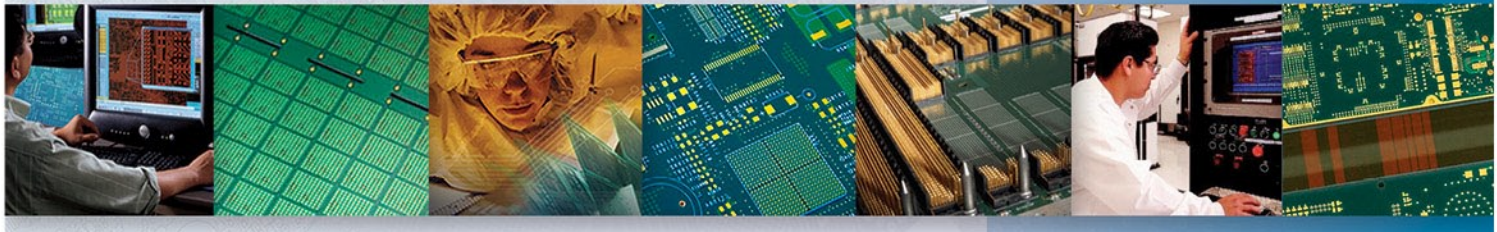

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Adhesive Delamination

by Paul Reid
PWB INTERCONNECT SOLUTIONS

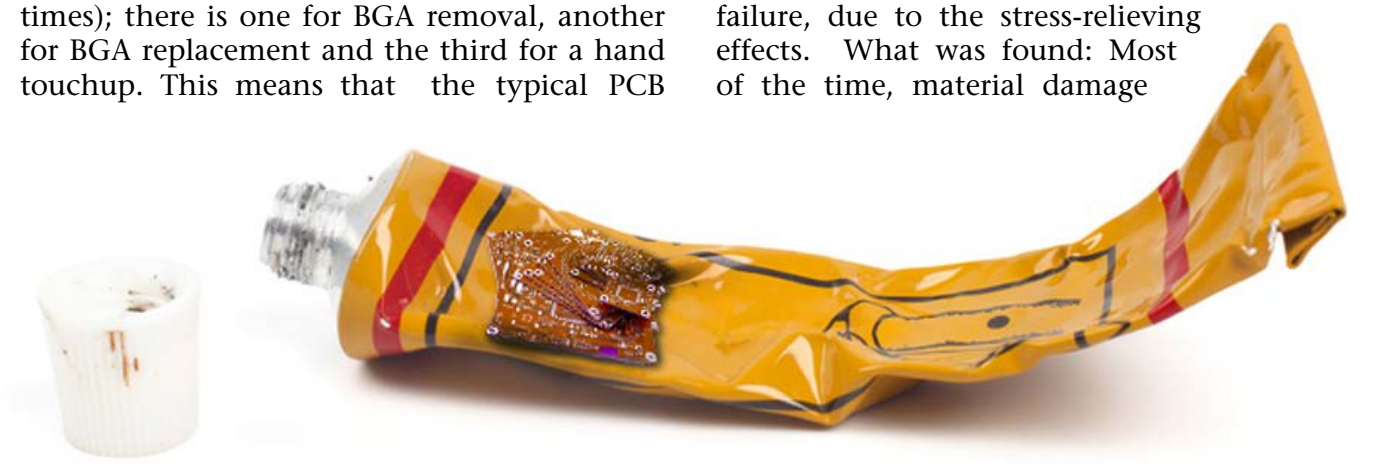
SUMMARY: With the advent of the European Union's Restriction on Hazardous Substances (RoHS) legislation, lead was removed from solder. This required PCB assembly temperatures to be increased to accommodate the higher melting point of the lead-free solder alloys. The assembly temperature increased from a traditional level of 230°C, up to a maximum of 260°C, although some assembly houses are able to assemble at a more modest 245°C.

The additional 30°C has been demonstrated to negatively impact the dielectric material within most types of PCBs used in electronic products. Many of the commercially available dielectric materials are not guaranteed to remain robust in HDI applications when exposed to multiple 260°C assembly and rework thermal excursions. The higher assembly and rework temperature are increasing the risk of material damage.

The lead-free assembly processes typically takes two or three thermal excursions to 260°C. There are commonly two thermal excursions in a reflow oven for double-sided assembly and one for localized attachment, plus a wave soldering if connectors are installed. Rework can add another two or three thermal excursions (usually at higher temperatures for longer times); there is one for BGA removal, another for BGA replacement and the third for a hand touchup. This means that the typical PCB assembly (PCBA) may be required to "survive" six high-temperature thermal excursions.

It is not fully understood whether materials used in HDI applications can withstand that amount of heat multiple times without experiencing some level of material degradation. Consequently, material damage is becoming more common in HDI applications where the assembly temperature is applied with 260°C as the upper requirement. In a recent study, 15 out of 24 electronics-industry-approved, lead-free compatible materials exhibited material damage after six assembly cycles to 260°C in a conventional reflow oven.

Thermal cycle testing was done on representative coupons to determine PTH reliability and material robustness. The thermal cycling method used is known as interconnect stress testing (IST). In this method, the thermal cycling of IST coupons ranges from ambient to 150°C in three minutes and returned to ambient in approximately two minutes, whilst constant monitoring of the resistance in copper circuits is recorded. The thermal excursions precipitate barrel cracking that result in increases in the resistance in the test circuit. A 10% increase in a circuit's resistance is considered a failure (IPC standard). Any material damage present can artificially extend thermal cycles to failure, due to the stress-relieving effects. What was found: Most of the time, material damage



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ADHESIVE DELAMINATION *continues*

stress relieves the interconnections – for example, in the central zone of the PTH barrel – thus extending the thermal cycles to failure. This was not commonly found when coupons are exposed to 6X230°C preconditioning, but it is more common when similar coupons are exposed to 6X260°C.

For example, coupons were tested as received without preconditioning and achieved a mean of 500 thermal cycles to failure. When similar coupons are exposed to 6X230°C preconditioning, they failed with a mean of 375 cycles to failure. When the coupons from the same group were exposed to 6X260°C they would fail with a mean of 500 cycles to failure, which was counterintuitive. When the 6X260°C coupons were microsectioned, they exhibited material damage while the coupons tested as received and those exposed to 6X230°C showed no material damage. What was called for was a means of finding material damage electronically.

One finds material damage in IST coupons by through the use of DELAM circuits that are built into the coupons. What we do is measure changes in capacitance. The design of the coupon is such that there is a flooded ground plane wherever there is a ground plane on the circuit board. With this design, one can measure the capacitance between these ground plane layers. Typically, the capacitance is measured to be 100 to 400 picofarads between ground planes in IST coupons. What we do is to measure the capacitance before preconditioning, after preconditioning, and at end of test. Greater than a -4% reduction in capacitance suggests that there is significant material damage. A cross-section is then processed on the coupons in question to confirm or refute the presence of material damage. If there material damage is confirmed, then the threshold stays at -4%. If the microsection refutes the presence of material damage, the threshold is reduced to -6%. In this way, one knows generally at what layers the material damage occurs and which coupons to microsection. Typically, one or two coupons show material damage per group of six. Rarely does one find 100% of the coupons showing material damage. By processing the coupons in this way, we greatly increase the ability to find and understand how, when, and where material damage occurs.

Based on our DELAM method, the material damage may be classified in four category types: adhesive delamination, cohesive failure, crazing, and material decomposition. Each of these types has characteristics that are unique unto themselves. This column is focused on adhesive delamination; we will cover the other three types of material damage in future columns.

Adhesive delamination is a breakdown between two laminated interfaces. This is the type of damage seen when two laminated surfaces come apart. There are three stages of dielectric material: A, B and C. The A-stage material is the uncured liquid epoxy. The B-stage material has been manufactured with glass fibers embedded in the epoxy, with or without copper foil on the outer layer, and the epoxy is partially cured and therefore a little bit tacky to the touch. The C-stage material is a fully cured epoxy, copper foil and fiberglass boards. During the fabrication of PCBs, fabricators use mostly C-stage and B-stage materials. During lamination, the B-stage layers become fully cured and as such are used to "glue" the other B-stage and C-stage layers together. The most common types of adhesive delamination are the breakdown between the B-stage and C-stage material, B-stage material and copper, and less frequently between epoxy and the glass bundles as a group.

There are three stages of dielectric material: A, B and C. The A-stage material is the uncured liquid epoxy. The B-stage material has been manufactured with glass fibers embedded in the epoxy, with or without copper foil on the outer layer, and the epoxy is partially cured and therefore a little bit tacky to the touch. The C-stage material is a fully cured epoxy, copper foil and fiberglass boards.

In adhesive delamination, it is the laminat-

ed surfaces that come apart. One cause of adhesive delamination is weaknesses between the epoxy and the oxide coating on the copper. The copper is frequently oxidized to improve adherence between the copper and the B-stage epoxy. Years ago, the amount of oxide coating played a large role in adhesive delamination. If the amount of oxide coating was too thin, then there was a tendency toward adhesive delamination. If the oxide coating was too thick, there was also a tendency to delaminate. This was one of the reasons for IPC's TM 650 method 2.4.24.1 Time to Delamination (TMA Method) – 12/94 test to see if the oxide coating would delaminate or not. The T260°C test works by bringing a small sample of the material to an isotherm of 260°C, measures the thickness of the sample and hold it there until a delamination causes the thickness to increase, or for 10 minutes, which was end of the test.

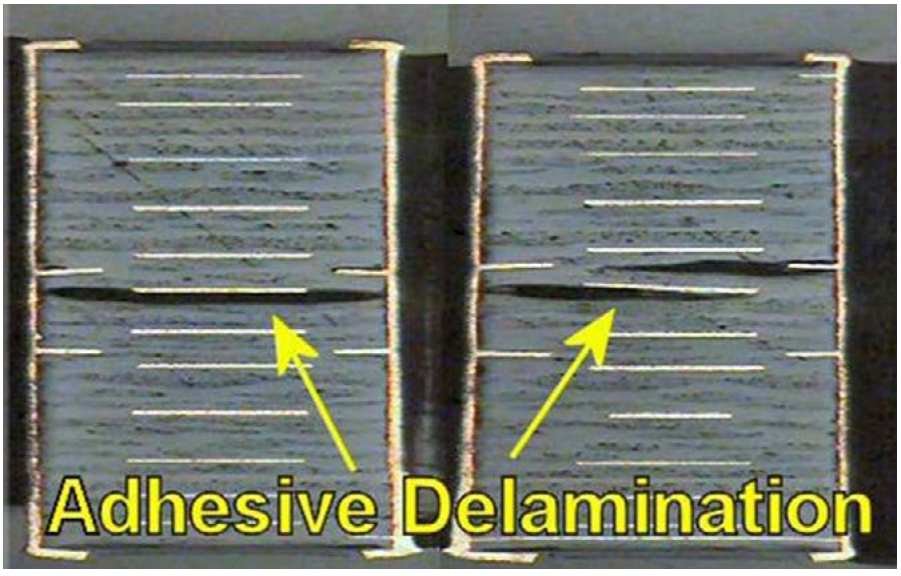

Figure 1: Cross-section showing adhesive delamination.

Another test, IPC TM 650 2.4.13.1 Thermal Stress of Laminates – 12/94 was the solder float test. In the test a sample of the board or a coupon is floated in solder for 10 seconds, then microsectioned and examined for material damage. This T260 test and solder float test became the quintessential material tests for material reliability. We find that neither of these tests anticipates delamination of materials. These tests were useful when materials had a low T_g, but do not anticipate material damage in higher-T_g materials available today. Today's oxide treatments are greatly improved and tend not be so prone to delamination.

One of the considerations related to adhesive delamination is vapor pressure. What happens is that the water and other volatiles trapped in the material exert pressure when the water vaporizes into steam. The vapor pressure of water is 300 pounds per square inch (PSI) at 230°C and is 700 PSI at 260°C. So logically, the water vapor should produce huge amounts of pressure internally in the PCB. But we forget to take into account the amount of water available. Given that the amount of water is so low in circuit boards, as low as 0.12% of the weight of the board (polyimide could be as high as 4%), all the water vaporizes and then the pressure stops rising at such a significant rate. This limited amount of water limits the pressure that the water exerts on in the board.

Generally the water vapor and the pressure generated from the water is not enough to cause the PCB to undergo adhesive delamination. There must be other factors at play besides the vapor pressure of the water or other volatiles. Let's say you have adhesive delamination in a group of coupons that were not dehydrated by baking before preconditioning. In order to save them, you decide to bake the rest of the coupons at 105°C for four hours in an attempt to drive the water out of the coupons before preconditioning. The odds are that the coupons will still delaminate. I have never found that baking to remove water tips the scale and saves coupons from delaminating. In fact, the bake, if it is too aggressive, at too high a temperature or for too long, may force the coupons to delaminate sooner. The tendency to delaminate after aggressive baking may be due to thermal aging of the epoxy when exposed to high temperatures for long periods of time.

Adhesive delamination looks like a blister on a cross-sectional view (Figure 1). It is long

ADHESIVE DELAMINATION *continues*

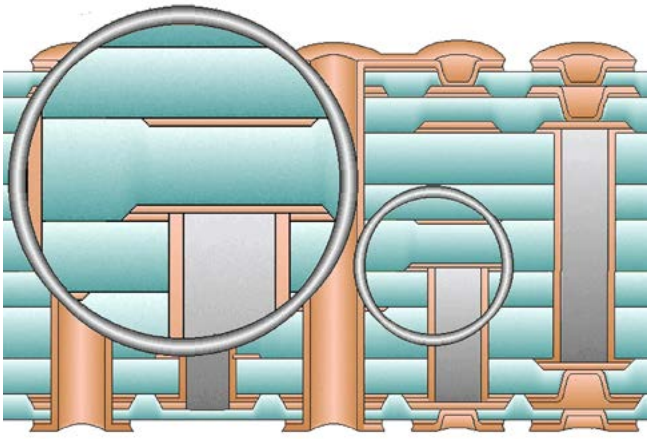

Figure 2: Animation depicting adhesive delamination.

and tapers to a point at the two ends. The delamination is along laminated surfaces like the interface between the B-stage and C-stage, B-stage and copper or along the glass bundles. Delamination along glass bundle it is not the individual glass fiber but between the glass bundles as a group and the adjacent epoxy. Crazing is a separation between individual glass fibers. The concepts associated with crazing will be covered in another column.

In adhesive delamination, the separation is along the laminated interface. Frequently this delamination is deep within the board and it is not visible by an external examination. Most often, this sort of material damage occurs during assembly and rework. This is more common with the thermal excursion associated lead-free assembly and rework. In the animation, notice that the delamination occurs during the heating cycle. **PCBDESIGN**

Paul Reid is program coordinator at PWB Interconnect Solutions, where his duties include reliability testing, failure analysis, material analysis, and PWB reliability consulting.

IPC Sees Bright Future for Latin American Industry

Latin America is showing a new resilience and faster economic growth, which may make it an attractive region for investment, according to Latin America: Regional Outlook for the Electronics Industry, a new report published by IPC—Association Connecting Electronics Industries®.

"The Latin American region has received significant attention in the last few years as a potential growth area for the electronics industry," says Sree Bhagwat, IPC market research manager. "This report not only provides insight into the economy and prominent industry sectors, it also examines political, economic and business risks companies need to understand as they consider pursuing opportunities in the region."

The report focuses on the region's eight largest markets--Brazil, Mexico, Argentina, Chile, Colombia, Venezuela, Peru, and Ecuador--which comprise 78% of Latin America's gross domestic product (GDP) and 70% of the region's population.

According to the report, OEMs have stepped up their investments and operations in Latin America, most notably in the automotive industry, and manufacturing production is poised for solid growth in 2013. In addition, multinational corporations in Latin America are diversifying their investments from assembly production into research and development, aiming to gain a firm foothold in the market. The region's consumer markets are also expanding, driven by strengthening currencies, advanced credit, and improved credit conditions.

Latin America: Regional Outlook for the Electronics Industry is 44 pages long and includes data on economic indicators, forecasts for 2013, expert commentary and illustrative charts and graphs. IPC members may purchase the report for $475; the standard industry price is $950.

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Most-Read News Highlights from PCBDesign007 this Month

① SiSoft, Tektronix Bridge Simulation and Measurement Gap

SiSoft is collaborating with Tektronix to bring full support for silicon-specific IP models developed using the IBIS-AMI modeling standard to the SDLA Visualizer software package from Tektronix. This effort will ensure that lab measurements can be post-processed to accurately predict link behavior at physically inaccessible test points.

② Mentor Celebrates 25 Years of HyperLynx With New Technology

Key features in the new HyperLynx product release include advanced 3D channel and trace modeling, improved DDR signoff verification, and accelerated simulation performance—up to 5X faster. Engineers and designers who use the HyperLynx products during the system design process can quickly analyze potential high-speed design issues that can impact signal integrity, power integrity, and EMI performance.

③ AWR, Zuken Team on RF Verification for PCB Design

The new interface enables an intelligent, collaborative design flow for RF design and verification on the PCB. Users now have flexibility to bring in an entire design, or select specific RF signals and other design structures to conduct electromagnetic analysis.

④ Intercept Celebrates its 30th Anniversary

Founded in 1983, Intercept began as a consulting firm performing electrical engineering-related software and hardware projects. During the company's first 10 years, the issues with CAE and CAD software were so apparent that the firm began developing its own EDA software. Pantheon PCB design software was first released to the public in 1994, and quickly became a success in the EDA market.

5 IPC Design Standard Tackles Technologies, Techniques

The newly revised IPC-2221B, "Generic Standard on Printed Board Design," provides a basis for the design of all types of printed boards and addresses areas as diverse as testing, via protection, test coupon designs and surface finishes.

6 Ucamco Unveils Ucam 10.1

Ucamco has unveiled a new suite of CAM solutions. Ucam 10.1 delivers a range of new and enhanced tools and functions, unleashing unprecedented engineering software capabilities and allowing incoming data to be entered into production with greater ease, speed, and accuracy.

7 PCB Design Software Market Shows CAGR of 5.3%

The global PCB design software market has witnessed an increasing availability of cloud-based PCB design software. However, the availability of open-source PCB design software could present a challenge to the growth of this market.

8 EDA Consortium: PCB & MCM Revenue Up 9% in Q3

EDA Consortium's Market Statistics Service reports that EDA industry revenue increased 4.9% for Q3 2012 to $1.62 billion, compared to $1.54 billion in Q3 2011. PCB and MCM revenue of $153.0 million represents an increase of 9% compared to Q3 2011. The four-quarters moving average for PCB & MCM decreased 1.7%.

9 DesignCon 2013 Concludes with 8% Growth in Attendance

"DesignCon 2013 was a great success," said Wendy Yamaguma, Senior Events Director, UBM Tech Electronics. "Attendance was up, spirits were high, and we have already begun to receive excellent feedback about our content, events, speakers, and services."

10 Cadence Reports Revenue Increase in Q4

Cadence reported fourth quarter 2012 revenue of $346 million, compared to revenue of $308 million reported for the same period in 2011. Revenue for 2012 totaled $1.326 billion, compared to revenue of $1.150 billion for 2011.

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February 26-28, 2013
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February 26-28, 2013
Stuttgart, Germany

IEEE CPMT Advanced Pkg Material
February 27-March 1, 2013
Irvine, California, USA

Medical Devices Summit
February 28-March 1, 2013
Boston, Massachusetts, USA

Executive Briefing: Thermal Management Market Vision & Strategies
March 18, 2013
San Jose, California, USA

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March 19-21, 2013.
Shanghai, China

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Next Month in *The PCB Design Magazine*

Decades after designers supposedly embraced DFM techniques, CAM departments are still busy decoding designers' intent. In the March issue of *The PCB Design Magazine,* we'll drill down into DFM and try to find out why designers and fabricators so often talk past each other. And don't miss our special post-show coverage of IPC APEX EXPO and The Designers Forum.

See you in March!