THE pcb design MAGAZINE

April 2013

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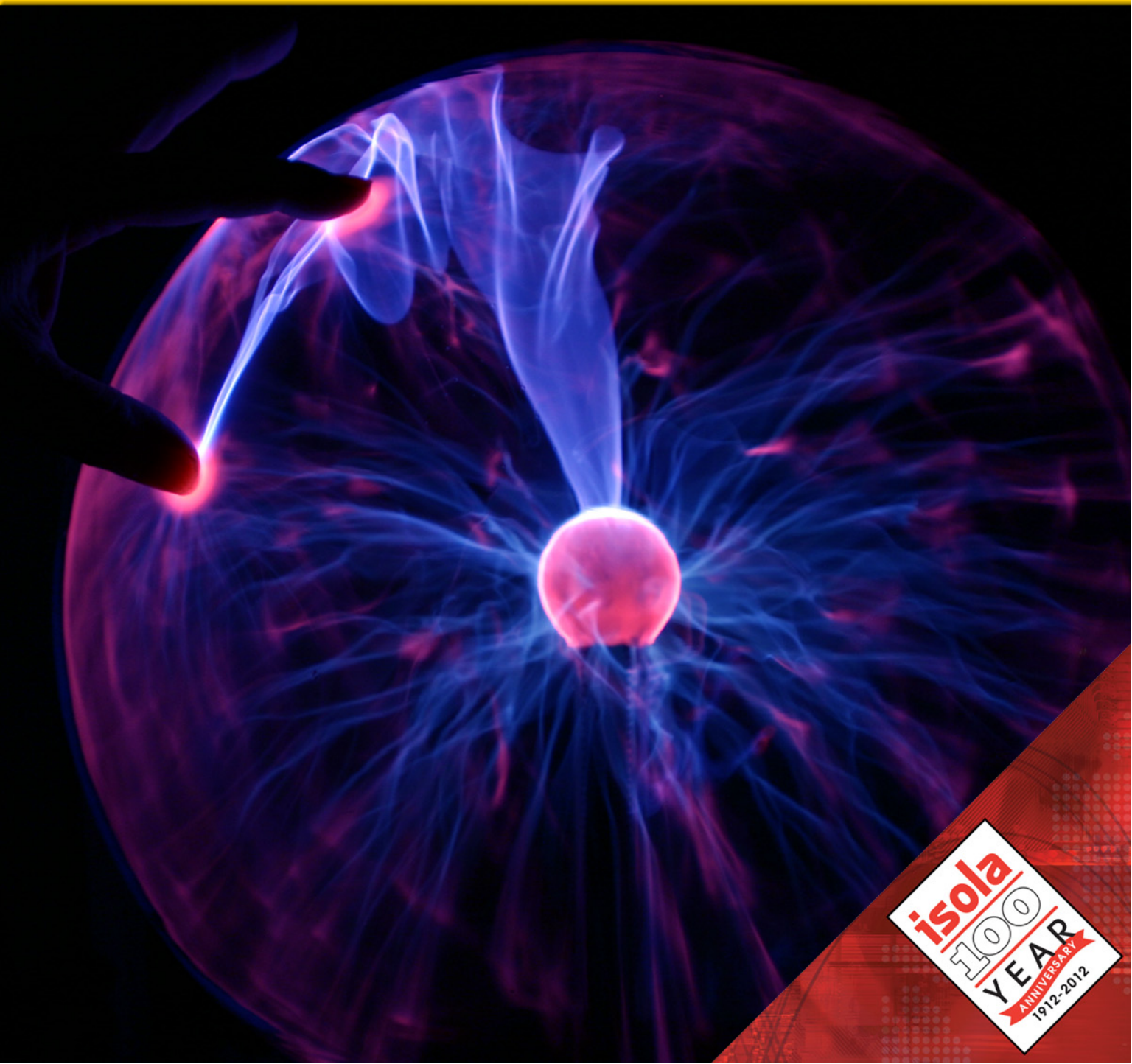
EMI / EMC



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THIS ISSUE: EMI & EMC

FEATURED CONTENT

Radiated emissions can cause a variety of problems on your PCB – even if you're designing boards with "mature" technologies. In this issue, our columnists and contributors tackle the challenges of achieving EMC and discuss some proven methods for minimizing EMI transmissions from the ground up.

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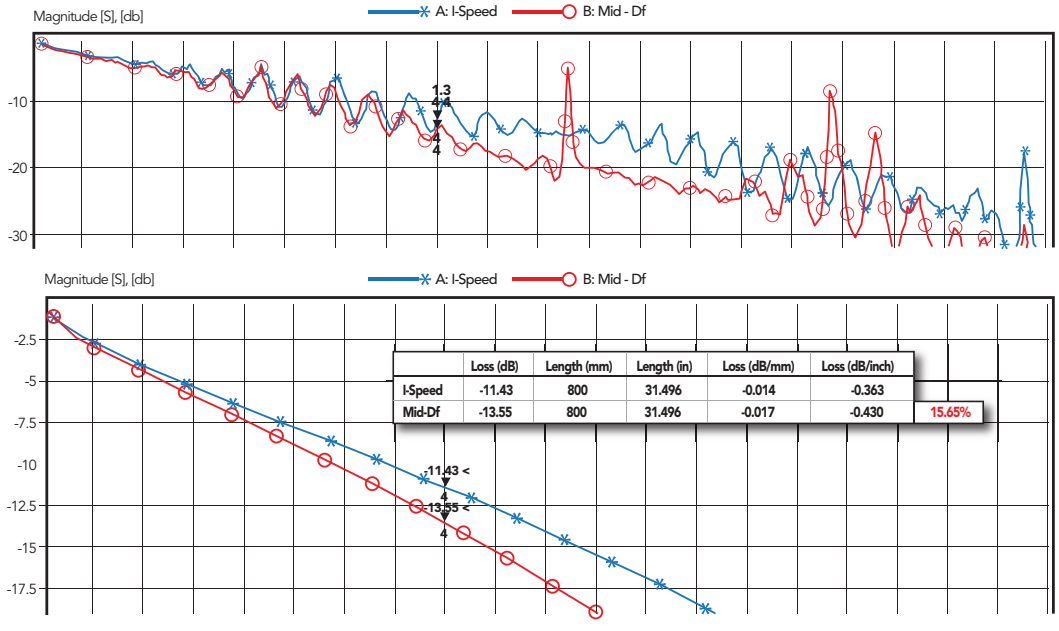

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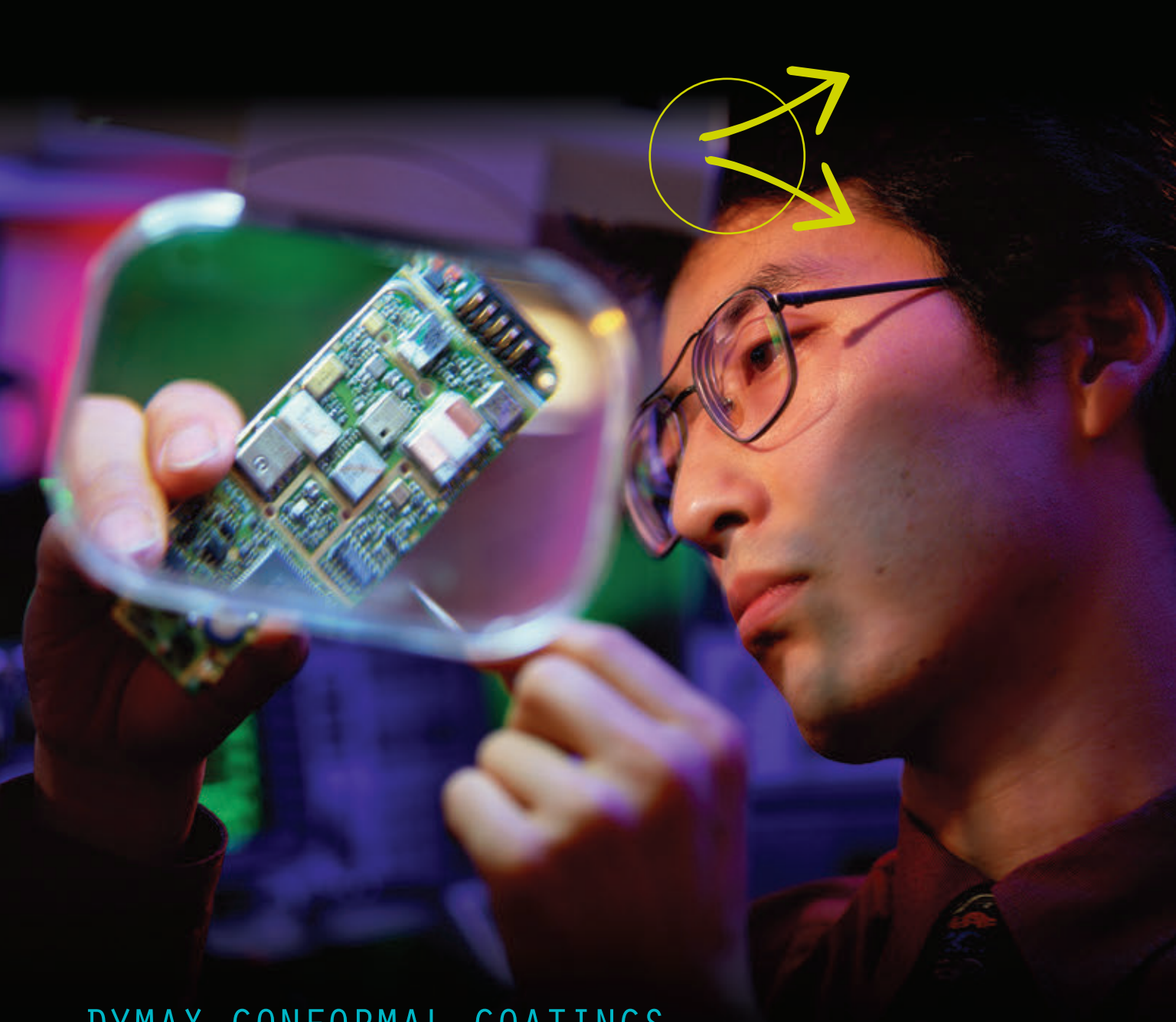

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THE SHAUGHNESSY REPORT

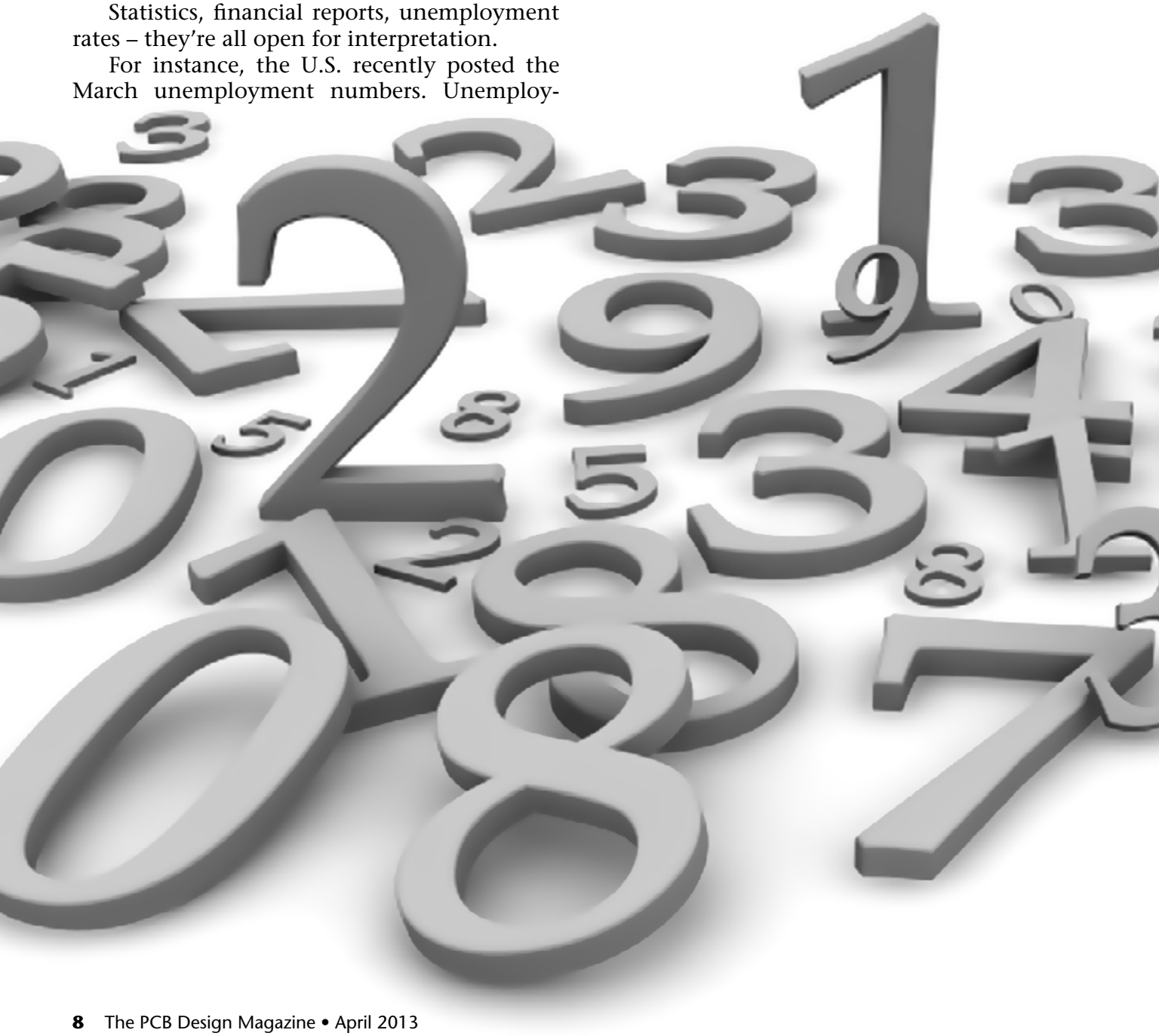
By The Numbers

by Andy Shaughnessy
I-CONNECT007

When I bought my first car that required monthly payments, my dad co-signed for the loan. The salesman tried some financial sleight-of-hand, and then announced, "Figures don't lie." My dad, whose first new car was a 1949 Ford, answered, "Figures don't lie, but liars do figure."

Statistics, financial reports, unemployment rates – they're all open for interpretation.

For instance, the U.S. recently posted the March unemployment numbers. Unemployment fell to 7.6%, which is great news. Or is it? The percentage of able-bodied "potential" workers actually working is lower than any time in the last 34 years – 63%. People who give up on looking for a job don't count toward the final jobless head count.



Still, a 7.6% unemployment rate is better than the 8-9% rates of a few years ago. But it all depends on whether you want to see good news or bad. I think any analysts or news anchors looking for causal relationships between these numbers and, say, an administration's economic policy may be trying to solve an equation with too many variables.

Worse, these monthly job reports don't tell us much specifically about those who design and manufacture electronics. It takes six months for the Bureau of Labor Statistics to break down various occupations' jobs data by geography, mean salary, etc.

Every so often I visit the Bureau of Labor Statistics website. I recently pored over the site, hoping to find some concrete, unambiguous jobs data regarding those who design or manufacture electronics. The BLS site has a cornucopia of interesting, cross-referenced data, if you know how to search for it. (Plus, I just like data and surveys. I even read the methodology behind polls used in political campaigns.)

The first problem: BLS has almost no concrete data about PCB design or designers. No matter how I searched, I found nothing about PCB designers, design engineers, or circuit engineers. We've all seen now how hard it is to quantify the number of PCB designers in the US or worldwide. Well, to the BLS, the entire PCB industry is nearly invisible. More accurately, the info is hidden in plain sight among larger industries, and delineated by final product

There was, however, a lot of data on electrical engineers; unfortunately, it includes EEs working at power plants and other careers not related to PCBs. But this will give us a good ballpark reference.

The May 2012 jobs data tells us that there were 160,560 EEs employed in the U.S. last spring. Their annual mean wage (found by adding the total salaries and dividing by the number of workers, in case you've blocked out everything you learned in your "sadistics" class) of $91,810 is about what we'd expect.

There were 12,960 EEs involved in "Semiconductor, and Other Electronic Component Manufacturing," earning an annual mean wage of $99,540. "Computer Systems Design and Related Services" totaled 4,520 EEs, earning an annual mean wage of $102,860.

The states with the highest EE employment:

1. California – 24,110
2. Texas – 11,840
3. New York – 9,120
4. Massachusetts – 7,520
5. Florida – 7,270

The states paying the highest EE salaries:

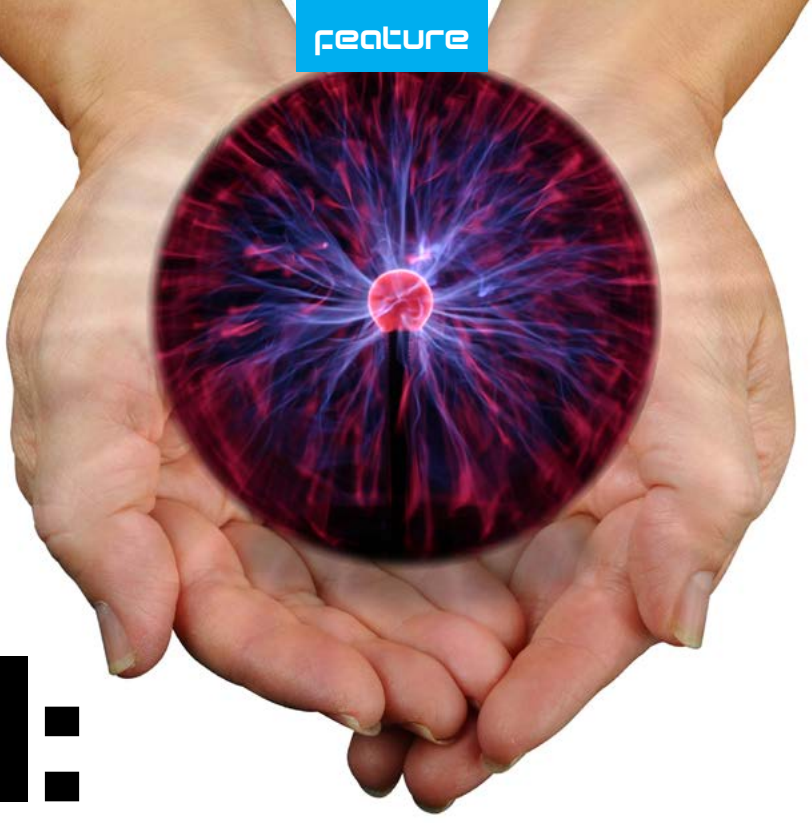
1. California – $107,280
2. Alaska – $104,360
3. District of Columbia – $104,040
4. Massachusetts – $101,750
5. Rhode Island – $97,760

Not surprisingly, the states paying the highest salaries have among the highest costs of living in the U.S. Also not surprisingly, San Jose rang up the highest annual mean wage for a metro area, $115,300, and the highest concentration of EE jobs – 6,920. Even after back-to-back recessions, Silicon Valley still employs more EEs than many states in the U.S. The No. 2 metro area for EE job concentration was Huntsville, Alabama, with 1,590, and No. 3 was the "Space Coast" area near Titusville, Florida, with 1,290.

Huntsville and the Space Coast both revolve around military contracts; it will be interesting to see if these areas lose EE jobs as a result of the sequestration. Sure, they're really just cutting the projected increase in government spending. But it would be foolish to think sequestration won't have an effect on PCB design and manufacturing down the road.

It's difficult to find concrete data for our industry, but I'd I recommend that everyone check out the Bureau of Labor Statistics site. Hopefully, there will be updated EE numbers soon. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.



EMI:

What It is, Where It Comes From and How to Control It

by Lee Ritchey
SPEEDING EDGE

SUMMARY: There are a variety of technical books that address EMI and EMC. However, none of them really gets down to the basics of where EMI comes from, what it really is, why it is an issue and what to do about it.

There seems to be a great deal of mystery surrounding EMI and EMC. I have a shelf full of books on the subject. Some of them are technically very good and at least three of them are so full of misinformation that their followers are more likely to have EMI problems than if they did nothing. Of the books that are technically very good, all describe at great length how to measure near field and far field emissions and how to calibrate measurement setups.

However, none of them really gets down to the basics of where EMI comes from, what it really is, why it is an issue and what to do about it.

Electromagnetic interference (EMI) is electromagnetic energy that escapes one product and interferes with another. This can happen in two ways. First, electromagnetic energy can be radiated into space because there is an accidental antenna extending from the product. Second, the energy can be conducted out of the power lines of the product and into the power terminals of another product.

Conducted EMI is measured in the band of frequencies from 150 KHz to 30 MHz and radiated EMI is measured in the band of frequencies from 30 MHz to 1 GHz or to 5x the highest clock frequency, whichever is higher.

Electromagnetic compatibility (EMC) refers to a product that has been designed so that it is not interfered with by other products as a result of electromagnetic radiation or conduction. In other words, noise in the form of electromagnetic radiation coming from another source that can cause a product to malfunction does not affect it.

Understanding EMI

Starting with radiated EMI, I find it easiest to understand this energy by looking at it as an unwanted radio link. The same mechanism that makes a radio transmitter and receiver pair work is in effect when there is an EMI problem. Looking at what is needed for a good radio link helps understand what needs to be done to eliminate an EMI problem.

There are two necessary elements in a good radio transmitter, which is what we have when a product is failing EMI tests. These are a source of RF energy (transmitter), and a radiating surface

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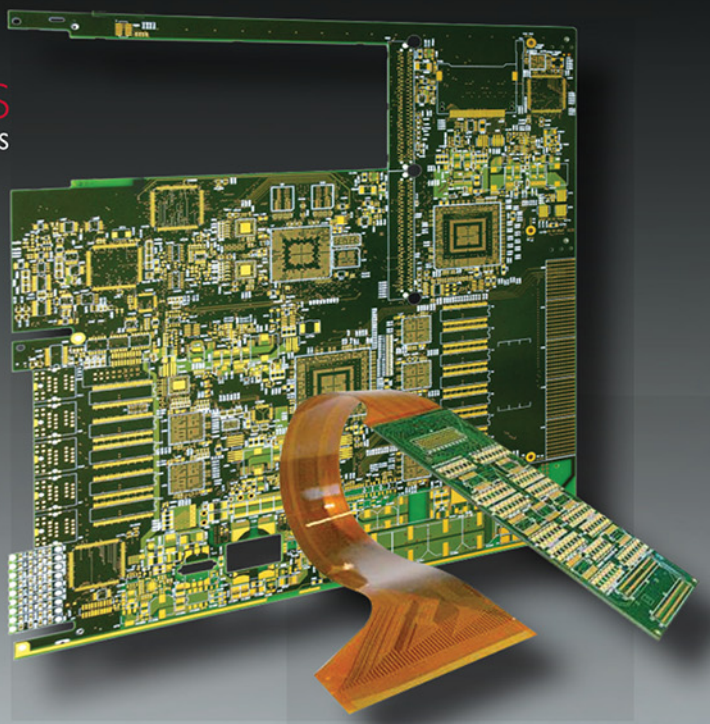

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(antenna). If I remove either one, the source of EMI or the radio signal is removed. Controlling EMI consists of eliminating either the source or the antenna.

The rule of thumb methods passed around the engineering community tend to focus on removing the source of EMI. These methods evolved in the 1980s, when the operating frequencies of products were well below the 30 MHz starting point for measuring EMI. At that time, occasionally ASICs would have speeds fast enough to generate noise in the 30 MHz to 1 GHz range. Inserting a ferrite bead in the power lead of such a device prevented it from operating fast enough to cause EMI. Such techniques focus on removing the source.

Modern electronics operate well above the 30 MHz starting point for measuring radiated EMI. As a result, suppressing EMI with ferrite beads and other similar methods by preventing circuits from operating at high frequencies is not a choice. This leaves only one alternative – eliminating accidental antennas.

There are many speculations about what can make a good antenna. One that is commonly passed around is that traces on outer layers of PCBs can cause EMI. It is easy to demonstrate that this is not so[1]. Antennae are bidirectional. This means that an antenna that is good at receiving is equally good at transmitting and vice versa. One way to demonstrate that antennas or traces close to planes don't work well as antennas is to take a handheld AM radio tuned to a weak station. Move it close to a sheet of metal such as the planes in a PCB. The signal will fade away, even though the antenna is still some distance from the plane.

What Makes a Good Antenna for Radiating EMI?

Stated simply, things that make good antennas are objects that stick up above the PCB (e.g., PLCC lead frames and other elements that leave the PCB, such as unshielded wires going to mice and monitors, etc.). Things that don't make good antennas are things that don't stick up, such as traces on a PCB. Two PCBs joined by a connector, such as a DIMM connector, form a dipole antenna that works very well. PGAs and BGAs in sockets also make good antennas.

Points to remember:

- A two-board set will usually behave as a dipole antenna.
- An unshielded wire leaving a Faraday cage will be an antenna.
- Connecting logic ground to a Faraday cage in more than one place often turns the cage into an antenna.
- A component lead frame protruding above a PCB is an antenna.
- Cutting ground planes can turn a PCB into a dipole antenna.
- Connecting plug-in module face plates to logic ground turns the faceplate into an antenna.

Three Treatments of Antennas

There are three ways to treat potential antennas. These include:

- Shield them when they leave the product.
- Place a low-pass filter in series with the antenna where it leaves the product.
- Place the product in a Faraday cage.

Placing a low-pass filter on a wire as it exits a product is an effective way to prevent noise from getting onto the wire. For a low-pass filter to be effective it needs to produce substantial attenuation from 30 MHz to 1 GHz. Such a filter will need to be made from very low-inductance capacitors in order to work across this range. The best capacitors for this purpose are formed from the planes of the PCB, and either fill in a signal layer or part of a plane borrowed for this purpose. Implied in the use of low-pass filters is the idea that the useful signals exiting the product on such a wire are well below the 30 MHz starting point for measuring EMI. The ferrite donuts surrounding the cables to displays and other peripherals are doing this low-pass filter job. On occasion, I have seen an EMI practitioner place a ferrite around a wire or cable, such as a USB port, where the useful signals are in the EMI band. This results in reducing EMI, but it also creates attenuation of the useful signal, sometimes to the point of causing a malfunction.

Shields on cables are a way to prevent a wire that leaves a product from becoming an anten-

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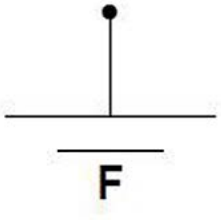
na. If the product does not have a Faraday cage (a metallic enclosure that surrounds a product that radiates energy in the EMI band), the shield needs to be tied to the logic ground of the PCB from which it exits. If the product is surrounded by a Faraday cage, the shield needs to be tied to the Faraday cage at the point where the wire exits. Shields are extensions of Faraday cages.

The Faraday cage reflects this energy back into the product. It rarely absorbs it. This is the ultimate method for containing EMI. It is necessary when a system has multiple PCBs or when there are large components sticking up that can serve as antennas. It should be pointed out that the Faraday cage itself can serve as antenna if the error is made to connect logic ground to the Faraday cage (some erroneously call it "chassis ground") at more than one place. The most common error of this type is to tie logic ground to the Faraday cage at the backplane of a system, and then to tie logic ground to the faceplates of the plug-in cards. A clue that this has happened is detecting EMI at the "cracks." I often hear this described as EMI "leaking out" at the cracks or seams of the box.

The Faraday cage usually is made up of parts of the chassis, such as the sides of a card cage. Because of this, the term "chassis ground" is often used when discussing EMI containment. It is confusing to use such terms, as they can mislead people. I use the term Faraday cage only when discussing EMI and represent it with this symbol:



True, some parts of the chassis are used to form part of the Faraday cage, but the "chassis" is not the EMI containment vessel.

The Source of EMI Energy

Traditional wisdom states that the system clock is the primary source of EMI. This was true long ago when the clock was the fastest signal in a product. However, this is not the case now and has not been so for quite some time. Figure 1 is the emissions spectrum for a dual-speed Ethernet interface card. The system clock is 33 MHz. None of the emissions in the spectrum are harmonics of the clock. Blue peaks are before adding plane capacitance and red peaks are after adding plane capacitance.

Notice that emissions are detected from about 30 MHz to over 1 GHz. Where are these signals coming from if not the clock? The answer is from ripple on Vcc due to inadequate bypassing. As can be seen from the paper by Todd Hubing[5], switching frequencies above about 100 MHz cannot be supplied or contained by discrete bypass capacitors because of their parasitic inductance. The source of energy to support switching events above 100 MHz is the capacitance formed by the parallel power planes. In the above design, there was very little capacitance between the power planes. This was remedied by filling in unused space in signal layers to form additional plane capacitance. The result cited above was caused by this increase in plane capacitance. There is no other way to reduce emissions in the EMI frequency band to a level where this product would pass.

The energy involved in the above failure came from the fact that switching events attempted to draw current from a power subsystem incapable of delivering it. This resulted in an excessive ripple voltage on Vdd. Logic lines connected to logic 1 in CMOS circuits are essentially shorted to Vdd. Any ripple or noise voltage on Vdd is conducted out on the wire and can radiate into space.

Figure 2 shows the switching voltage and current waveforms for a transmission line 12" long being driven by a 5 volt CMOS driver. The spectrum is a Fourier transform of the switching current waveform. Notice that this spectrum has frequency components from 85 MHz to about 900 MHz. The clock frequency is 30 MHz and there are no harmonics of the clock in this spectrum. If the power supply bypassing does not include sufficient plane capacitance to supply this current pulse, there will be a ripple voltage on Vdd that corresponds to it. This voltage waveform impressed on an antenna will result in emissions frequencies that match those

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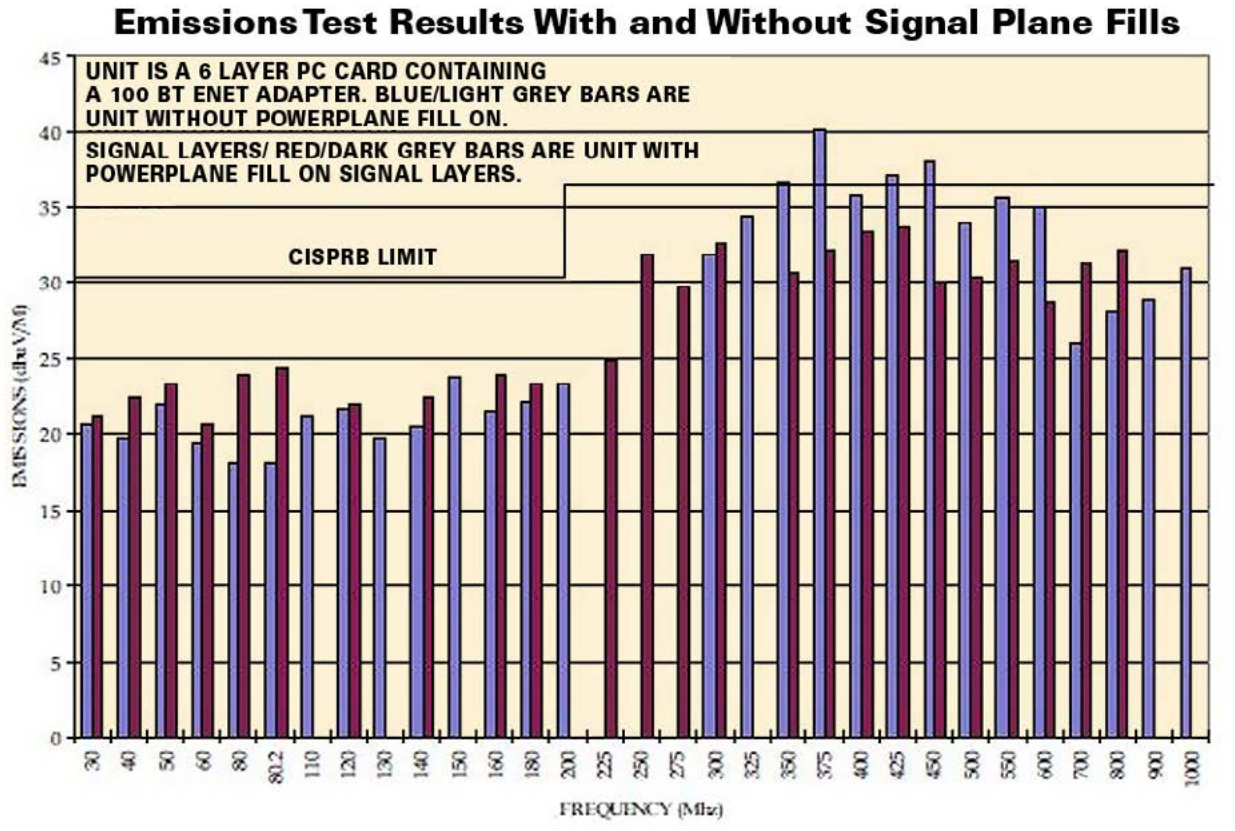

Figure 1: An emission scan of a dual-speed Ethernet card, before and after fix.

in the spectrum shown. Note: Todd Hubing's paper[5] demonstrates that plane capacitance is the supplier of current for frequencies above 100 MHz.

I have found that the best way to avoid EMI problems is by designing a bypassing scheme that minimizes ripple on Vdd. In fact, I have solved EMI problems, such as what is shown in Figure 1 by redesigning a PCB to improve the bypassing scheme. This involved adding enough plane capacitance to supply these high-frequency currents. Said another way, controlling EMI sources, ripple on Vdd being one of the biggest, is much less expensive than elaborate containment vessels. In the bargain, the circuits have better power sources and operate better.

Conducted EMI

Conducted EMI is energy that leaves a product through the power cord. The frequency spectrum of interest is 150 KHz to 30 MHz. This band of frequencies is well within the range of conventional components used to build low-pass filters such as inductors and capacitors. There is a wide range of such filters available for the manufacturers of DC-DC converters which can be inserted into the power lines as they enter or exit a product. For cost-sensitive products, it is often possible to build a low-pass filter from discrete components. In some cases, Ferrite toroids are clamped onto the power cord as it enters the product. This latter method is often found on low-cost products such as printers and monitors.

Beware EMI Rules of Thumb

A large body of information in circulation in the EMI community is flawed. I have watched some of these rules of thumb evolve when people who don't understand what really happens in high-speed circuits try to make up explanations for what is going on. This is the so called "it's magic" school of EMI control. In other cases, the rules appear to have been picked out of thin air.

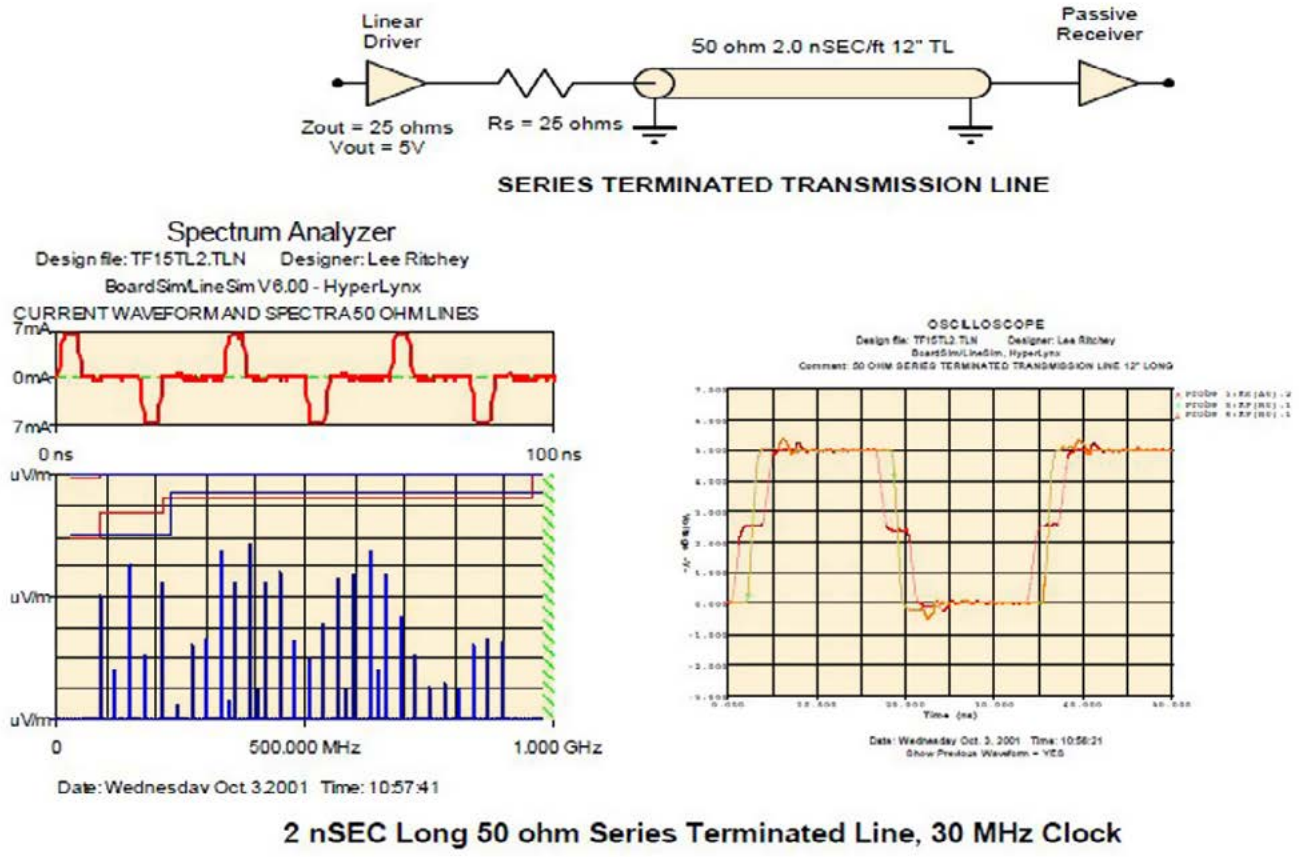

Figure 2: Switching waveforms for a 12" transmission line with frequency spectrum.

When I encounter a proponent of such rules and ask for the underlying research or testing that validates those rules, the reply is often "well, everybody knows that," "I'm the EMI expert and you have to believe these rules until you prove them wrong," or, "if you don't follow these rules, I won't guarantee your product will pass EMI tests." All of these replies leave me with an unsatisfied feeling. I have done testing to check them out, and time and again they have turned out to be invalid. In some cases, the rules do no harm. In others, they have the potential to cause operational failures. References 1 through 4 below are papers that test several of these rules of thumb to see if they are valid. They are all available on the Speeding Edge web site (www.speedingedge.com). I strongly suggest you download and read them.

As part of the testing I have done on this topic, I have learned that it is easy to demonstrate that good EMI rules are valid. When the proponent of an EMI rule cannot demonstrate its validity, it is wise to be suspicious of it.

Invalid EMI Rules

The following EMI rules of thumb have been proven invalid:

- Right angle bends in signal traces cause EMI[1]
- Traces on outer layers of PCBs cause EMI[1]
- Traces crossing splits in power planes cause EMI[2]
- Ferrite beads in the power leads of devices is an effective way to reduce EMI. This action can reduce EMI but at the expense of degrading the performance of the device. This should never be done.
- Recessing the Vdd plane in from the ground plane reduces EMI. This is the notorious 20H rule[3]
- Splitting ground planes eliminates EMI. This turns the PCB into a dipole antenna.

• Connecting logic ground to the "chassis" in multiple places eliminates EMI. This allows currents that should stay in the ground structure two choices of where to flow, the ground structure or the case work.

• The λ/20 rule. This rule states that logic ground should be connected to "chassis" ground at intervals of λ/20. Two assumptions have been made here. First, there is some frequency whose wavelength is λ/20 that is more important than the rest. Second, that this thing called "chassis" ground is somehow EMI-neutral. Both of these assumptions are flawed. Following this rule is a good way to create an EMI problem by turning the chassis into an antenna.

• Connecting bypass capacitors directly to the power pins of ICs reduces EMI.

• Plating the sides of a PCB is necessary to contain EMI. Just review how close energy stays to the trace it travels on and it can be seen that this energy won't "stray" out to the edge of the PCB.

• Rows of ground vias are needed around the edges of a PCB to contain EMI. See above.

• Place a strip of metal all around the edge of a PCB on both sides connected to ground to contain EMI.

• Flooding outer layers of a PCB with ground does not reduce EMI.

• Connecting logic ground to "chassis ground" with capacitors at the mounting screws does not affect EMI.

Can EMI Modeling Tools Predict EMI?

There is a desire to find some modeling tool that can look at a potential design and predict where EMI may come from in order to allow changes to be made that will guarantee successful emissions testing. This is a noble goal. Unfortunately, it is well beyond the reach of any tools that are available on the market or are likely to be made available in the foreseeable future. If one looks at the complexity of the problem, it becomes clear why this is true. Implied in this goal is the ability to build a 3D model of the functioning product and then analyze it as it performs through the frequency band from 30 MHz to 1 GHz in three dimensions. This is a colossal task!

If Modeling Doesn't Work, What Does?

I have found that focusing on making very good power subsystems and making a good environment for transmission lines is the best practice. This minimizes the sources and the antennas. If the product has two PCBs joined by a connector or cable, it will need to be in a Faraday cage. Managing the antennas that leave the Faraday cage is an integral part of this task. **PCBDESIGN**

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7. Ritchey, Lee W. and Zasio, John J. *Right the First Time: A Practical Handbook on High Speed PCB and System Design,* Speeding Edge, 2003.

Note: I have not listed the three books with the large number of errors and bad rules of thumb in them. Anyone wishing to obtain their names in order to avoid purchasing them can contact me through the web site, www.speedingedge.com.

Lee Ritchey is founder and president of Speeding Edge. A longtime PCB design instructor and consultant, Ritchey is the author of Right the First Time: A Practical Handbook of High-Speed PCB and System Design.

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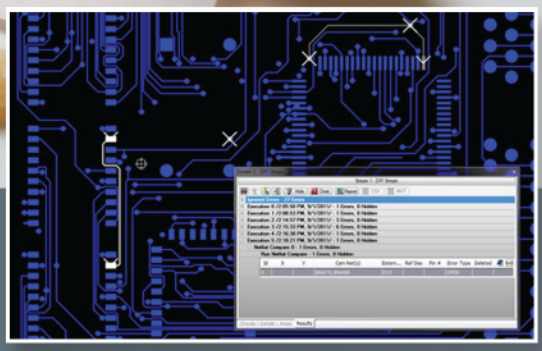
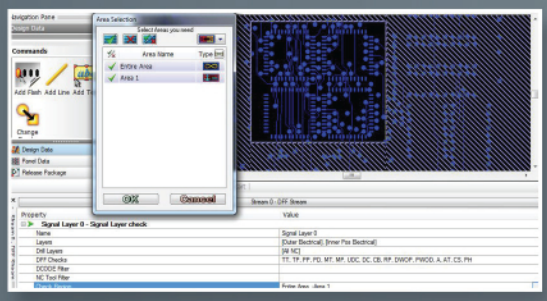


Netlist errors are quickly validated in DFMStream



Define DFM checks by area so components such as BGAs can be verified with unique rules different from rest of design

DownStream Technologies

A Small Leak Can Sink a Great Ship:

EMC Behavior of Traces Crossing Split Planes, Part I

Ralf Bruening
ZUKEN

SUMMARY: Laying out a trace across a split or gap with reference planes is a major EMC design rule violation. But often, PCB designers have no alternative other than to place some signals that cross cutouts, gaps or voids underneath or above the routing path.

It has been known for several years, discussed regularly in all the relevant high-speed design books and found in practically all PCB design guidelines – a trace crossing a split or gap with reference planes is a major EMC design rule violation. Ignore this and you could significantly impact the return current and the noise behavior of the PCB.

Many of today's electronics contain large ICs, such as FPGAs, ASICs or off-the-shelf processors that use multiple voltage rails. To maintain control over manufacturing costs, few electronic designers can afford to use the space for a full reference layer to support all the required voltage rails, including the reference planes to support the needed return path. Often, designers have no alternative other than to place some signals that cross cutouts, gaps or voids underneath or above the routing path.

But what might be considered a small design rule violation can impact the signal integrity behavior of single-ended and differential signals, as well as the overall EMC fingerprints of the PCBs. Violations like this increase the chance that the entire system will fail EMC testing.

When reviewing possible violations, it's important to understand the difference between the behaviors of single-ended lines and coupled

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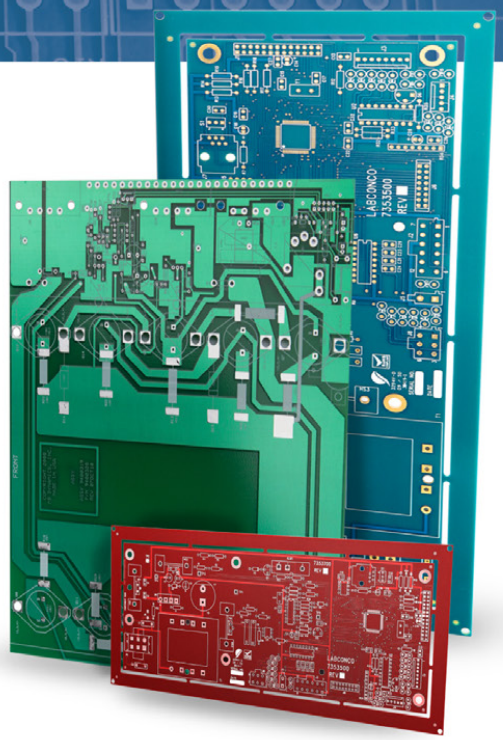

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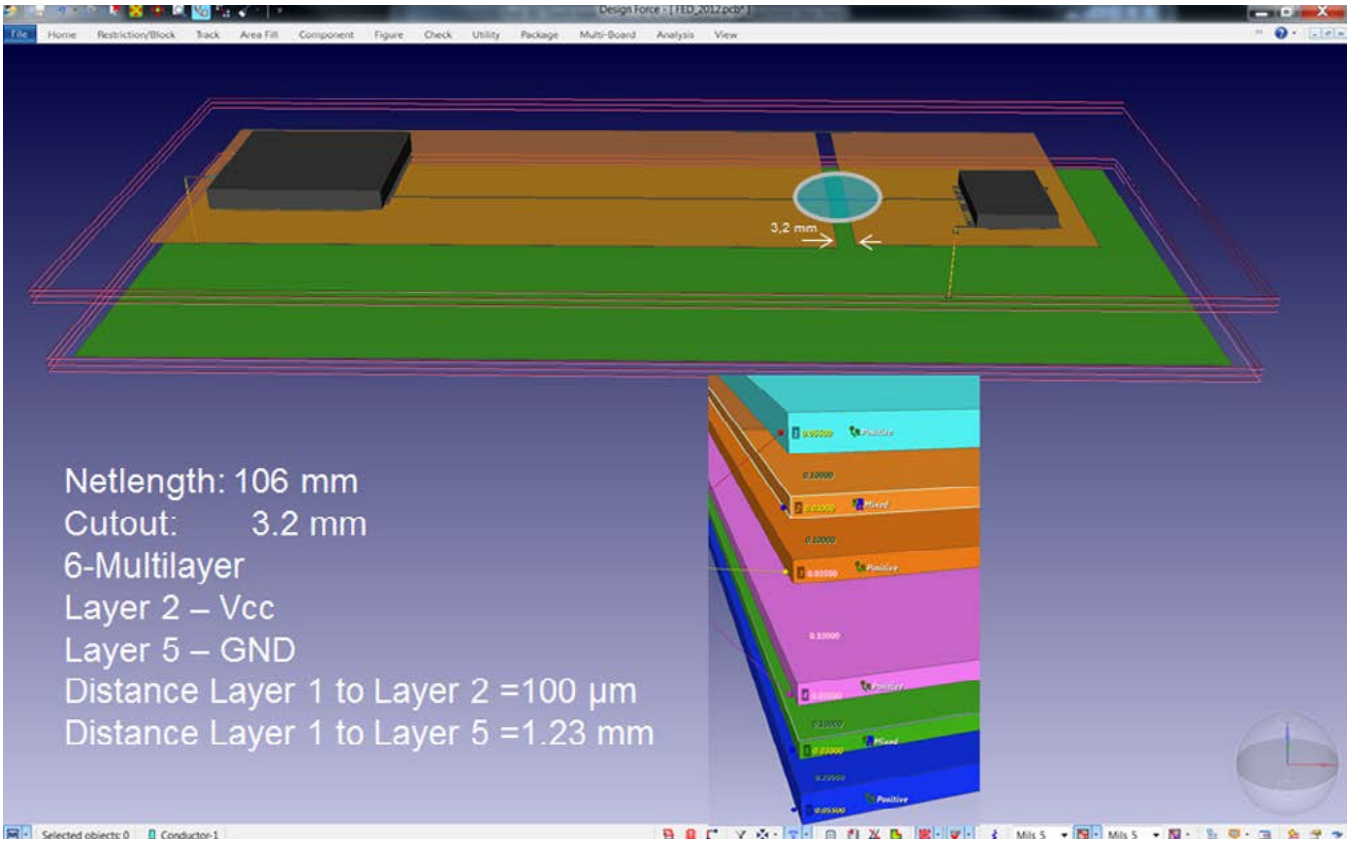


Figure 1: Signal crossing a split plane and board stack-up details in 3D within CR-8000 Design Force.

differential lines (which are commonly mistaken as immune to "bad" routing). Also, we need to study each case and the resulting impact on the design-related signal quality and EMC in terms of reflection, crosstalk levels, and the frequency domain behavior for resulting EMC far-field effects.

So let's start by doing a forensic study of a single trace crossing a split plane like the one shown in Figure 1.

In this case we have a single-ended track on a small test design crossing a gap over a small distance of 3.2 mm. This can be easily extracted into an SI model to compare one signal with that small gap-crossing segment and the other signal without it. From there, the engineer can analyze the effect on the signal.

As you might expect, the quality of the signal that crosses the gap is affected. The ringing increases by 200 mV, which is significant for a 1.8V DDR3 output driver.

Signal quality is only one small piece of the overall puzzle; since the signal switching for the logic levels is still within specification, you may assume that the impact is minimal and may be ignored. This may be true, but if we look more closely at the receiver switching, we will detect that there is a significant skew difference introduced by the small area crossing the gap, resulting in a skew difference up to 18ps on the receiver device.

When measuring signal timing with respect to voltage, a common rule of thumb is to allow 10% of the rise time as a margin. This example includes a fast DDR3 buffer (a Freescale DDR3 driver and Micron memory modules modeled by IBIS models). Following the 10% rule and considering that we have a buffer switching in the range of 270ps rise/fall time, this small routing mistake uses up a serious amount of the overall timing margin to cross the gap.

Now that we have looked at the signal integrity aspect of this for single-ended trace, let's look at the EMC footprint that results from this

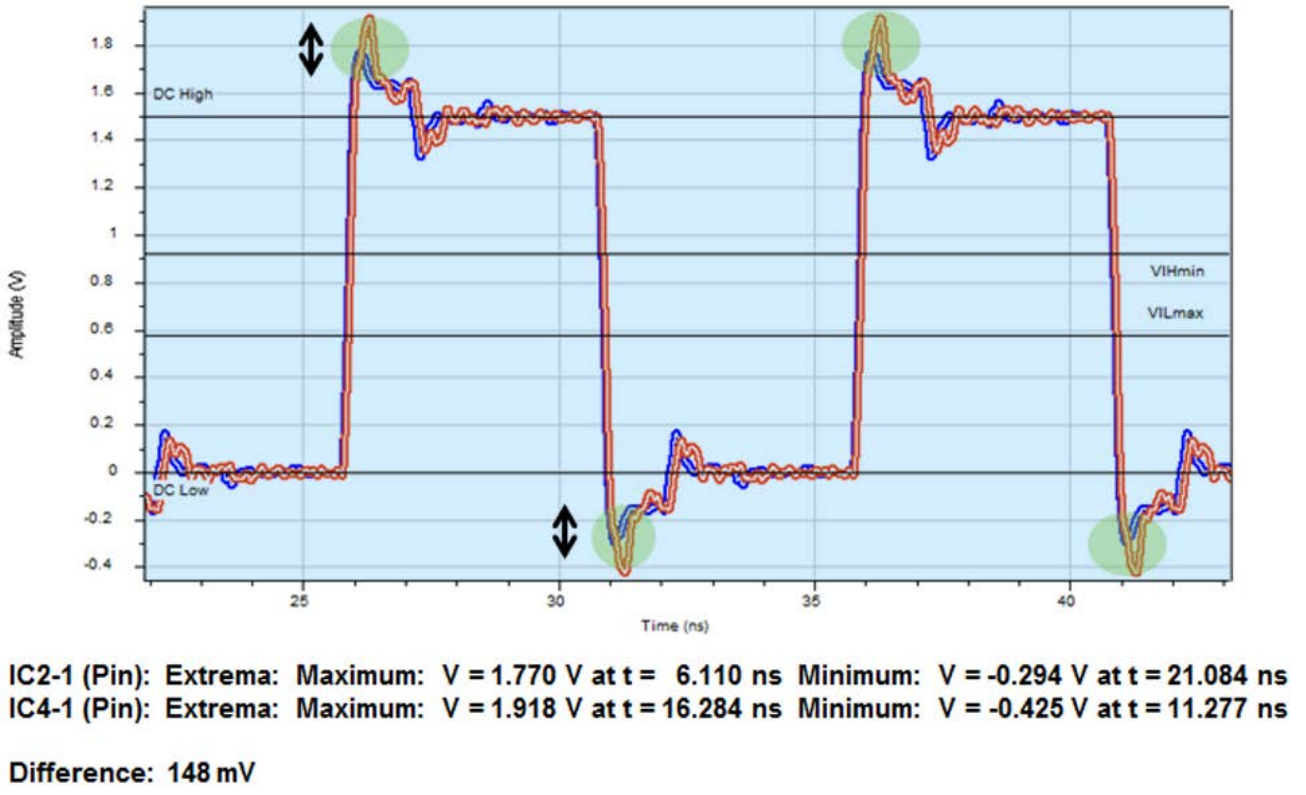


Figure 2: Comparison of voltage difference at the receiver for a signal with and without a cutout in the reference plane.

routing pattern. We know that the overall signal return path will increase due to the routing area crossing the gap. This will create quite an effective differential mode antenna where we can either use full-wave 3D solvers to precisely compute the electrical and magnetic field quantities, or we can use a max-emission calculator to quickly quantify the effects. (The calculator was developed by the EMC-Expert System Consortium at Missouri University of Science and Technology, formerly University of Missouri-Rolla.) The max-emission method is effective in capturing the efficiency of such PCB structure antennas, and is computed very quickly for any kind of routing patterns. The equation in Figure 4 is used to calculate the field strength of these antennas.

When applying this type of worst-case EMC emission analysis to a PCB structure with and without the signal pattern crossing the gap, you can expect the results illustrated in Figure 5.

So far we have looked at an individual signal line. On our example boards there are no single traces, but rather coupled signals that interfere with one another creating capacitive and inductive crosstalk effects. Now we need to determine if the trace crossing the split plane also impacts the crosstalk behavior.

Take the following configuration as an example: We have two lengthy coupled traces crossing a split. With such a large coupled area we can expect a significant amount of crosstalk.

Let's take a new test case where only a small

$$E(f)_{V/m} \le \frac{Z_0 \pi I(f) A}{\lambda^2 R} = 1{,}316 \cdot 10^{-14} I(f) A f^2 \frac{1}{R}$$

R = The distance to the Antenna
A = Antenna size/area
f = frequency

Figure 4: Equation to estimate electrical field strength for differential-mode EMC emission.

A SMALL LEAK CAN SINK A GREAT SHIP *continues*

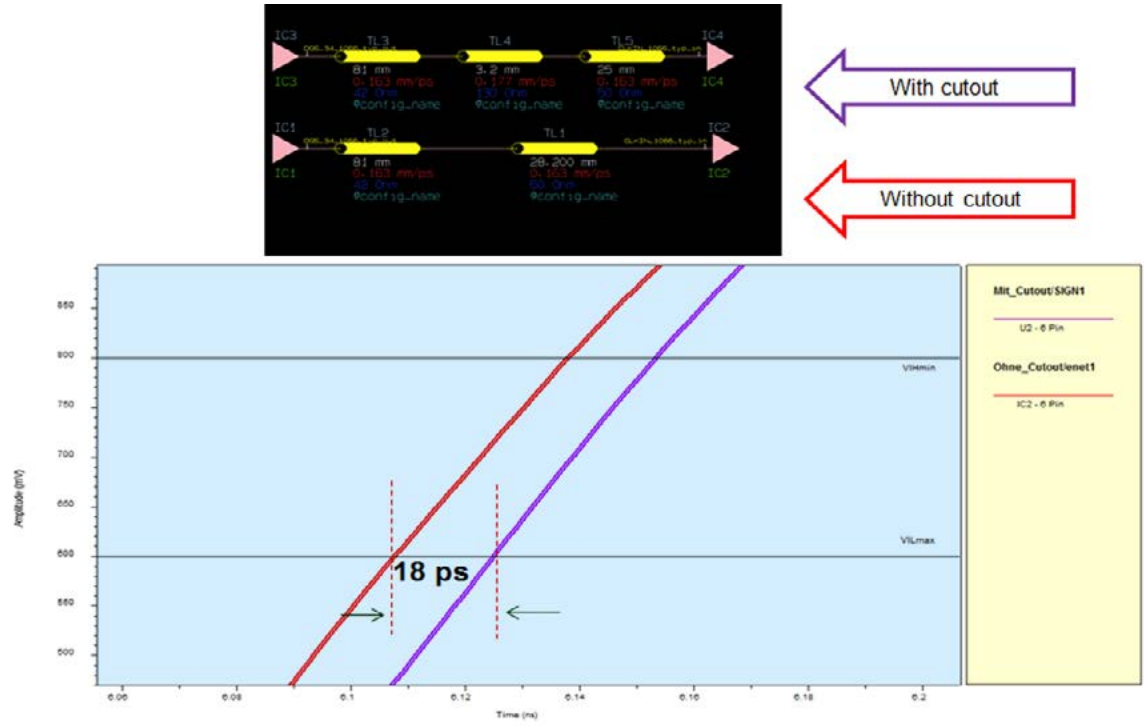


Figure 3: Difference in signal delay at the receiver.

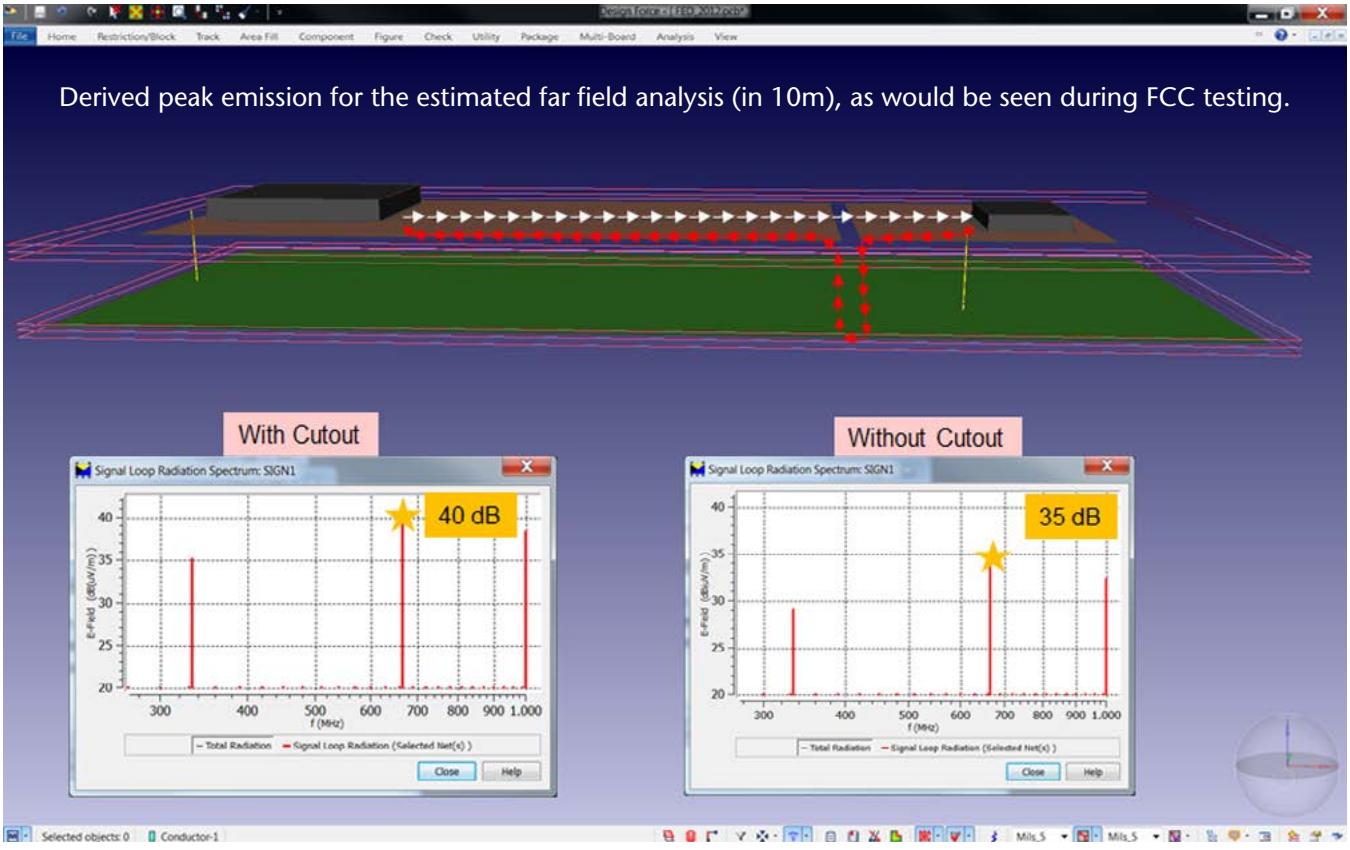


Figure 5: Estimated worst-case EMC emissions with and without reference plane cutout.

portion of the trace crosses the gap, we would expect to see less impact on the crosstalk voltages compared to a configuration that does not cross that gap. In both examples, a signal integrity simulator can help speed the design process by quickly computing voltage vs. time (note that coupled segments are shown in purple in the scratchpad editor, which depicts the extracted equivalent circuit model).

The result is rather surprising – we see in Figure 7 a significant increase in induced crosstalk with the traces crossing the cutout.

When comparing examples, the peak voltage of the example where the gap is crossed is nearly double that of the example without the gap.

So while it may seem minor, even a small design error on a single-ended trace can have significant impact on signal quality, timing, and EMC behavior. The result in our example shows a significant timing difference, double the amount of crosstalk voltage and a worst-case differential EMI of 5dbmV/m over frequency. How big are the margins in your designs? Designers should be aware of the possible pitfalls and decide on a case-by-case basis if the design stands up to the risks, or if they will "sink" the printed circuit board ship. **PCBDESIGN**

This article is the first in a two-part series by Ralf Bruening.

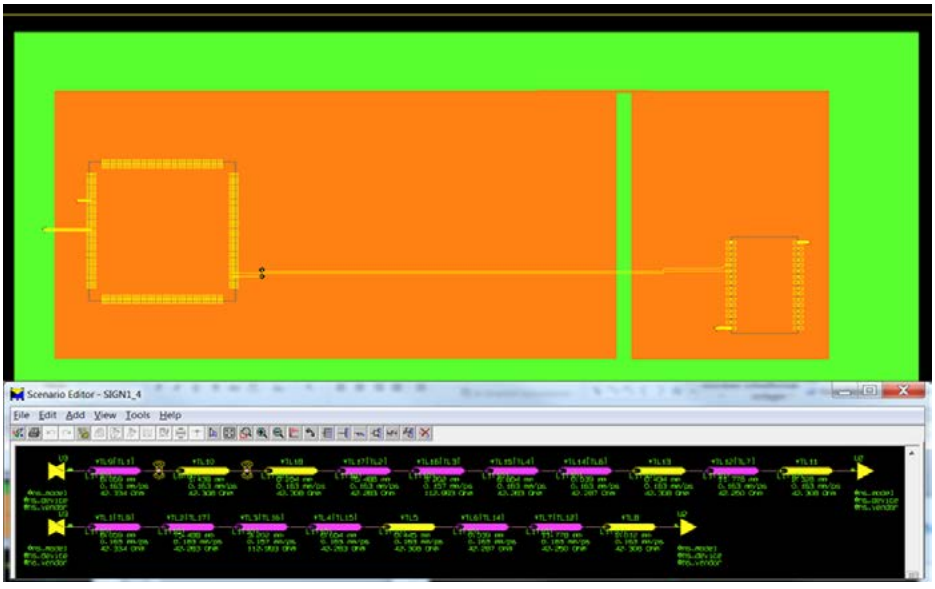


Figure 6: Schematic view derived from layout including coupled lines and equivalent circuit models for SI simulation.

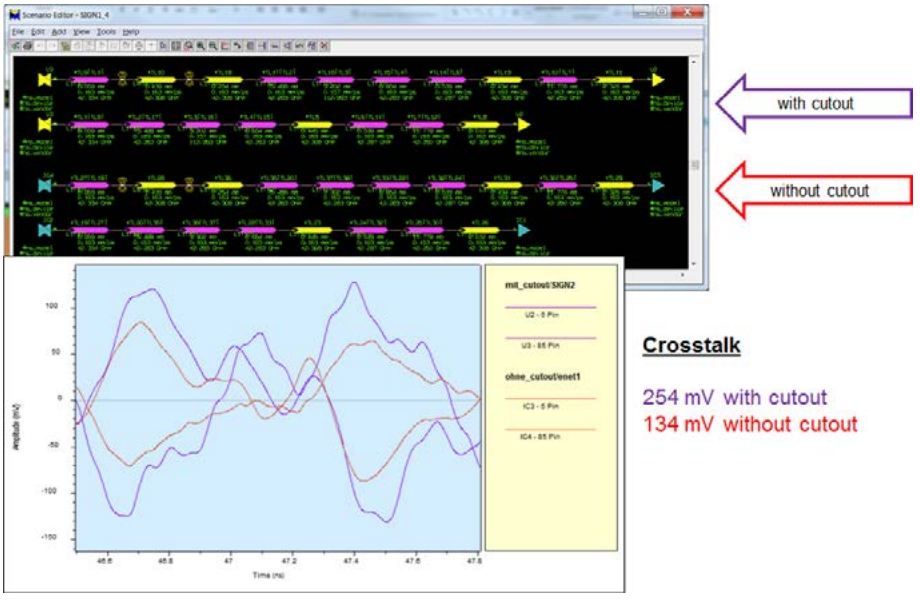
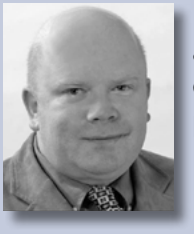


Figure 7: Comparison of driver and receiver crosstalk voltages, with and without the signal crossing the cutout.



Ralf Bruening is a product manager specializing in high-speed design, specifically signal and power integrity. He is based in Paderborn, Germany, at Zuken's EMC Technology Center.

The Advantages of CAD

by Jack Olson, CID+

SUMMARY: At this point in the story, the schematic has been packaged into the two types of data needed to start a circuit board layout: a part list and a net list. This month, Jack Olson offers a few final words about schematics and packaging and moves on to CAD libraries and PCB layout.

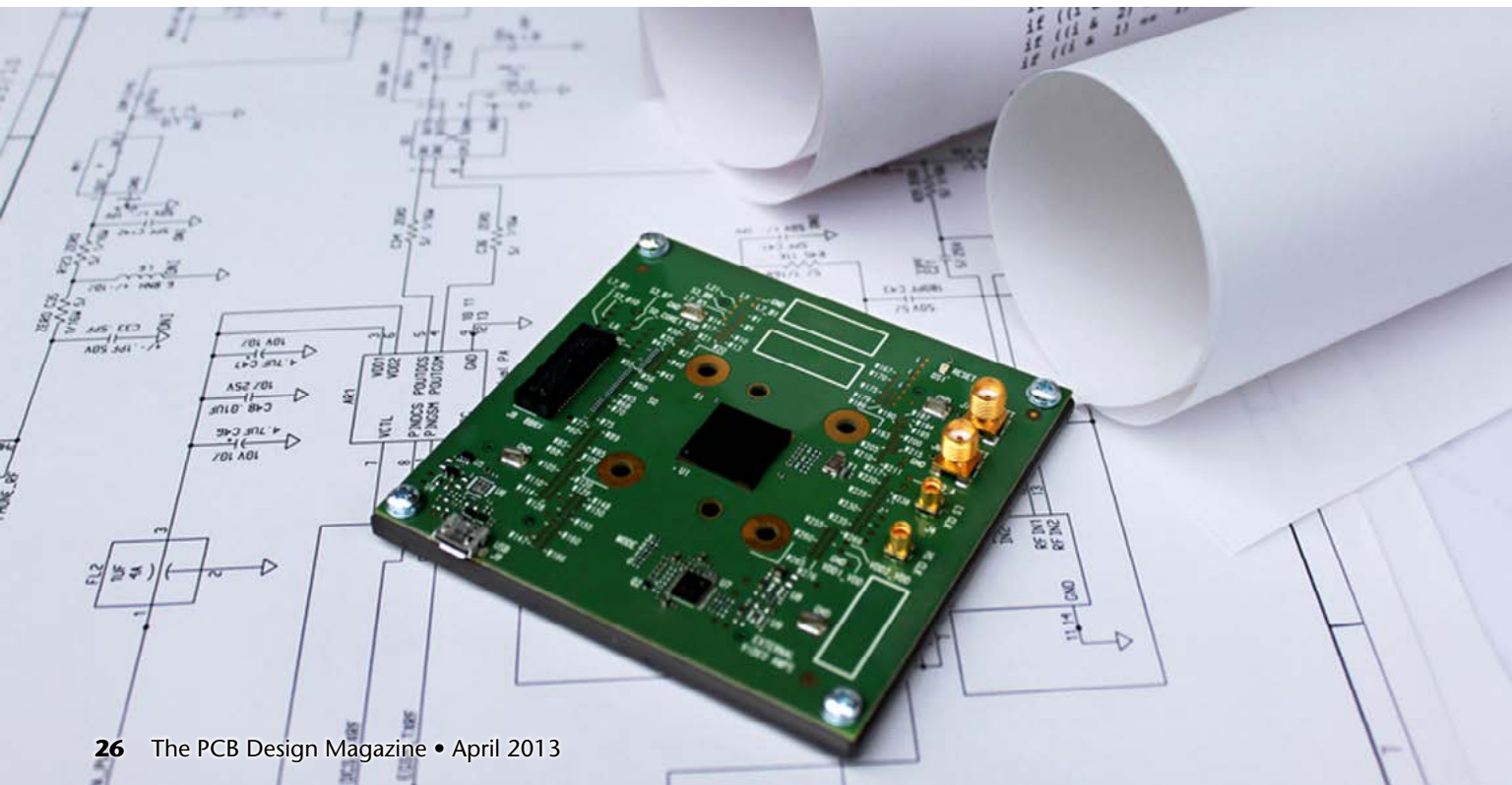
Schematic Capture

A schematic drawn on paper can be manually converted to a net list and part list to start a PCB layout, but from now on we'll turn our attention to circuit board design using computers. Most technical activities these days take advantage of the increased speed and accuracy of computer-aided design (CAD), so we'll leave the old methods for the historians to study. Software packages have been developed for electronics, and schematic concepts can be captured using a graphical user interface to do the following:

1. Select symbols from a CAD library
2. Place symbols on the screen
3. Connect the symbols together

You may not even need to assign reference designators or pin numbers to the symbols, unless you want to force specific arrangements (like connector pin assignments or logic gate assignments, for example) because the software can make these assignments automatically during the packaging process. The computer will or should make sure that each symbol is given a unique reference designator, assign pin numbers based on the selected component type, and report any conflicts or discrepancies. After the packaging process has been completed successfully, the schematic should be "back-annotated" with the pin number and reference designator assignments. Modern technology can provide assistance in other ways, too. For example, circuits can be moved, rotated or copied into many similar circuits with just a few mouse clicks.

Most CAD software packages also support the placement of standard drawing borders, title blocks and notes. If you can customize the title blocks and notes to meet the needs of your



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THE ADVANTAGES OF CAD *continues*

customer or the company you work for, you can save a lot of time when starting a new design. Sometimes these edited features can be saved as templates, allowing the library to store several variations for different customers or applications.

Net Properties

Take advantage of any support your software provides for assigning net properties, net classes or component grouping. If you can define circuits with unique group names in the schematic, it may make it easier to organize the design in PCB layout, by making it easier to collect related parts together for component placement. It might even provide a method of maintaining clearances or other types of rules that can be applied to groups. In most designs you will be using a default trace width for routing connections between component pins, but you may need to use a wider trace width for higher current requirements. This can be managed by assigning properties to specific nets. You will probably set a default minimum clearance between conductive features, but there may be higher voltages in some areas that require a greater clearance. If you can assign net properties or define net classes in the schematic, the requirements will be much easier to manage in the PCB layout.

Voltage clearances and current requirements are the most common types of net properties and are used in even the simplest designs, but there could be other considerations that should be defined using net class or net property attributes, if possible. High-speed lines will need

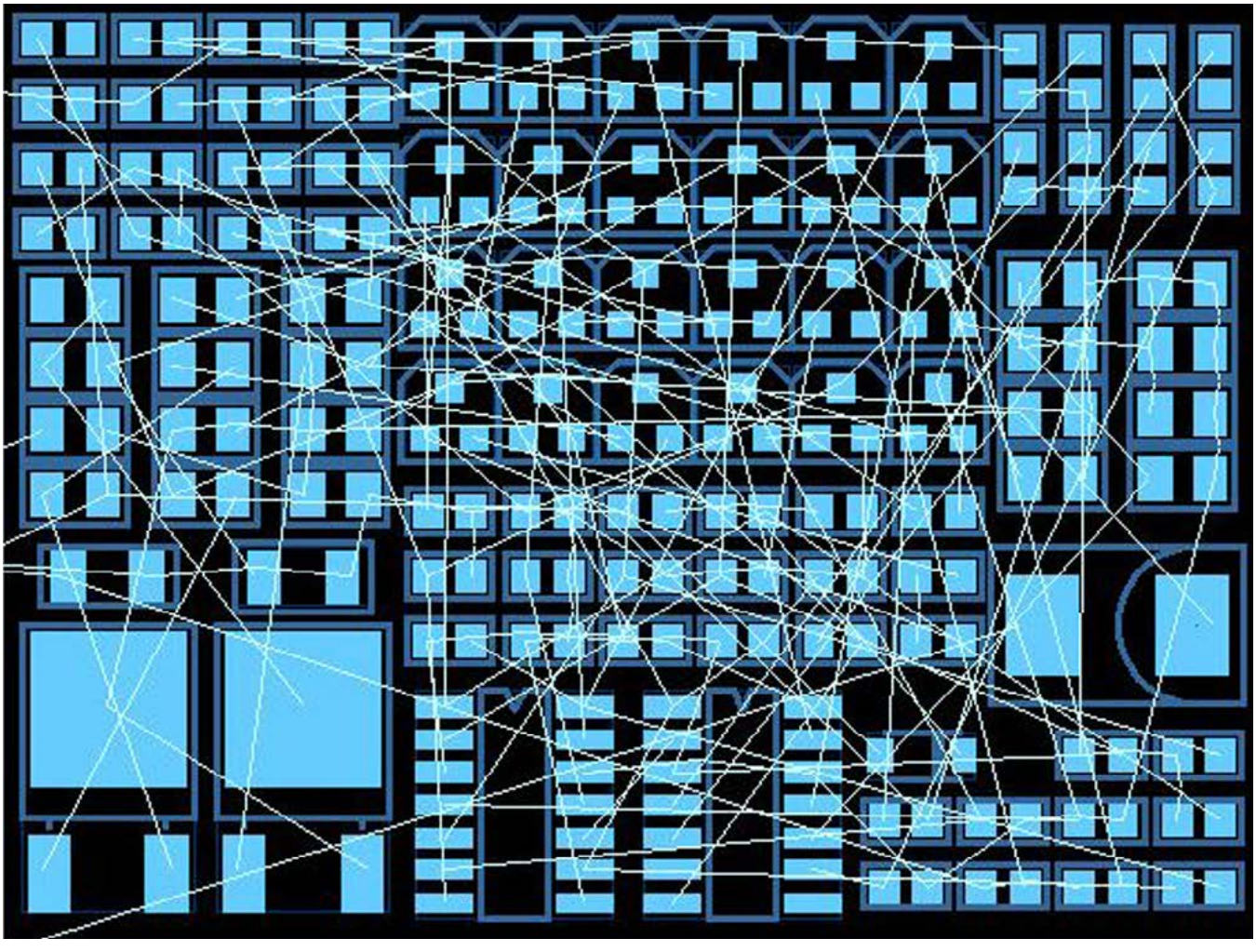

Figure 1: A rat's nest.

to be impedance controlled using specific conductor width settings. Noise-sensitive circuits or safety specifications could drive larger clearance requirements in some areas. Signal timing issues may drive trace length adjustments. Your design may eventually contain hundreds of different interrelated rules. Trying to manually check every rule in a complex design would be tedious and error-prone, so having the ability to embed them into the design, and having design rule check (DRC) software that can check them automatically can be real advantages. We may be good at pattern recognition and problem-solving, but computers are especially good at rule-checking. So to summarize, use the features provided by your software!

Trying to manually check every rule in a complex design would be tedious and error-prone, so having the ability to embed them into the design, and having design rule check (DRC) software that can check them automatically can be real advantages. We may be good at pattern recognition and problem-solving, but computers are especially good at rule-checking.

The Packaged Design

Now that we have a packaged PCB design database synchronized to a back-annotated schematic, we can begin the layout. Your software may provide a list of components to start placing, or it may just dump them randomly onto your screen for you to sort out. You might see all of the connections as lines from pin to pin; we call the view in Figure 1 a "rat's nest." You will eventually have to replace all of these lines with routed traces, adhering to the rules set for each net type.

I've mentioned before that the net list and part list are required to start a layout, but at this point the net connectivity will be maintained internally by the computer, and the physical part information will be drawn from a CAD library of "footprints" or "land patterns," so you won't strictly need them. You may want to export them as reports or as simple text files because they can be useful. Other people may need the part information for purchasing, as we've mentioned before. Send this information out as early as you can.

You should probably look through the net list at least once to check your net names. This can be important for designs that were packaged from large multi-sheet schematics, because it's easy to make a mistake from one sheet to another. If you named a net "+5V" on one sheet, and another sheet is labeled with "5V", they won't be connected in the layout. It will help if the list is alphabetized, so a discrepancy like two nets named "CLOCK" and "CLK" will be near each other, and you will notice them immediately. You may also see single-pin nets, which are nets that don't really go anywhere. Maybe you intended to connect the net on a different sheet and simply forgot about it, or used a different net name accidentally, but make sure to resolve any single-pin nets.

Finally, some CAD systems can report a list of spare gates. You will probably want to place spare gate symbols somewhere on your schematic (often on the last page) so you can tie unused inputs high or low. It will also be useful information for human readers later on if they need to use a spare gate for something.

If you make any final changes, make sure you repackage the schematic again to keep it "in sync" with the layout, or use the ECO capabilities of your software to keep track of them automatically. **PCBDESIGN**

Jack Olson, C.I.D.+, has been designing circuit boards full-time for over 20 years. He would like to thank Mark Marano and Les Asato for their companionship, and for leading him to his career as a circuit board designer at Laser Precision Analytical. Contact Jack here.

Most-Read PCB007 News Highlights

Viasystems Q4 Results Hit by Fire in China Facility

CEO David M. Sindelar says, "I expect first quarter consolidated net sales to be similar to our fourth quarter result, as we will experience the seasonal declines associated with the Chinese new year holiday and will be in the process of ramping production in our Guangzhou facility now that it has resumed full operations during the first quarter."

IPC: PCB Shipments Down 1.1% in January

"The book-to-bill ratio for the North American PCB industry strengthened for the second consecutive month, turning the corner in December after an eight-month downturn," according to Sharon Starr, IPC director of market research. "Sales and orders, however, remained sluggish in January."

CODI (Advanced Circuits) Posts $5.2 Million Q4 Loss

Alan Offenberg, CEO of Compass Group Diversified Holdings LLC, stated, "We are pleased to post strong operating results for the fourth quarter and full year 2012. CODI's cash flow for the three and 12 months ended December 31, 2012 increased YoY by 38.6% and 12.6%, respectively."

IPC's PCB Market Report Predicts Growth for N.A. Market

The North American PCB Market Report, published this week by IPC, predicts a modest return to growth in the North American PCB market in 2013. It also contains market data and a 2013 monthly sales forecast for rigid PCBs and flexible circuits.

TTM Restructures Equity Interest in DMC, SYE Plants

PCB manufacturer TTM Technologies Inc. has signed definitive agreements with its minority partner, Shengyi Technology Co. Ltd. (Sytech), to sell TTM's 70.2% equity interest in the SYE plant to Sytech and to acquire Sytech's 20% equity interest in the DMC plant.

Graphic Embeds RFID into PCBs

Graphic PLC presented a controversial paper at the EIPC Berlin Conference sharing information regarding its development project on embedding radio frequency identification (RFID) in collaboration with the University of Exeter.

Global PCB Industry's Growth Rate to Slow in 2013

In 2012, the global PCB industry saw a jump in terms of output value, benefiting from a rapid growth in shipments from Apple and Samsung, to 7% over 2011 levels to US $62B. The report sees no such possibility for such a large jump in 2013 and expects that the growth rate will slow to 2.7%.

Aspocomp Disappointed with 2012 Results

"2012 started reasonably well, but ended in disappointment. In spite of the acquisition of the Teuva plant, our net sales remained on par with the previous year. The second plant increased our indirect costs, depressing profit to EUR 0.6M, or 3% of net sales. Cash flow from operations was clearly in the black, around EUR 1.2 million," said Sami Holopainen, CEO.

IPC Conference to Focus on Big Picture

The need to look at the big picture or the whole electronic system rather than focusing on its individual parts is the impetus of the IPC Electronic System Technologies Conference and Exhibition (ESTC).

EIPC Endorses The PCB List

The EIPC writes in its endorsement, "The PCB List was created by I-Connect007/PCB007 as a tool for buyers and specifiers to quickly and easily find PCB manufacturers, anywhere in the world. We have reviewed The PCB List and it is indeed as stated, 'the world's most comprehensive online directory of PCB manufacturers, anywhere.'"

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Microwave Radiation Loss Concerns in PCBs

by John Coonrod
ROGERS CORPORATION

SUMMARY: A general definition of radiation loss is the energy on the circuit that is lost by radiating away from the circuit and into the surrounding environment. The lost energy has to go somewhere, and this can be a source of EMI issues. These losses become more prevalent at high frequencies, and designers must be aware of potential interactions between design techniques and circuit materials.

Circuits used at high frequencies, such as microwave frequencies, are prone to radiation losses. There are typically circuit design dependencies, but the circuit material may have an effect as well, and designers should be aware of potential interactions between the design techniques and circuit materials.

A typical PCB used at microwave frequencies experiences total loss, or insertion loss, made up of four different loss components: conductor, dielectric, leakage, and radiation losses. RF leakage losses at microwave frequencies are generally not an issue when using PCB materials; however, conductor losses and dielectric losses are definitely an issue. Radiation losses depend on the circuit configuration, design, material thickness, dielectric constant and frequency.

A general definition of radiation loss is the energy on the circuit that is lost by radiating away from the circuit and into the surrounding environment. The lost energy has to go somewhere, and this can be a source of EMI issues.

Impedance mismatches can be a significant source of radiation loss. Normally the designer will try to match impedances, but some scenarios in microwave design require different impedance levels. Another issue, which is sometimes related to impedance mismatch, is radiation loss due to signal launch. Signal launch happens where the connector meets the circuit board. In this area, the signal energy has to transition from the coaxial wave propagation mode of the connector to the planar mode of the PCB. The signal launch areas can have significant radiation loss and the microwave designer will typically put a lot of effort into trying to quiet that transition.

Circuit losses due to radiation are generally not an issue with stripline configurations, and can be much less of a concern with grounded coplanar constructions. The single-ended microstrip transmission line is more prone to radiation loss and there are several issues which

50 ohm microstrip, Dk=3.66, Df=0.0037, thickness=6.6mil

Freq (GHz)	Dielectric Loss (dB/in)	Conductor Loss (dB/in)	Radiation Loss (dB/in)	Total Loss (dB/in)
1	-0.012	-0.114	0.000	-0.127
5	-0.063	-0.284	-0.001	-0.349
10	-0.127	-0.408	-0.005	-0.540
15	-0.191	-0.503	-0.011	-0.705
20	-0.255	-0.583	-0.020	-0.859
25	-0.321	-0.654	-0.031	-1.007
30	-0.386	-0.718	-0.045	-1.151

50 ohm microstrip, Dk=3.66, Df=0.0037, thickness=20mil

Freq (GHz)	Dielectric Loss (dB/in)	Conductor Loss (dB/in)	Radiation Loss (dB/in)	Total Loss (dB/in)
1	-0.012	-0.037	0.000	-0.051
5	-0.064	-0.094	-0.011	-0.170
10	-0.130	-0.136	-0.046	-0.313
15	-0.198	-0.168	-0.103	-0.470
20	-0.268	-0.196	-0.183	-0.647
25	-0.339	-0.221	-0.284	-0.845
30	-0.413	-0.244	-0.407	-1.064

Figure 1: Comparison of losses for microstrip transmisison line circuits, of different thickness while using the same substrate material.

can vary the amount of loss. As general statements, a thicker circuit will have more radiation loss than a thinner circuit. A circuit with a low dielectric constant will have more radiation loss than a circuit with high dielectric constant. Applications operating at lower frequencies will have less radiation as compared to those at higher frequencies. Finally, there are interactions between all of these conditions, which can complicate the understanding of radiation loss in circuit designs.

To demonstrate some different scenarios, several examples will be given regarding radiation loss. The software modeling tool that will be utilized is MWI-2010, which is free to download here. This software can predict insertion loss of a microstrip circuit and show the different components of this loss.

The first example shows differences in radiation loss when using the same substrate, but at different thicknesses. Figure 1 illustrates a comparison in losses of two 50 ohm microstrip transmission line circuits built on the same high-frequency laminate. The first circuit is using a laminate of 6.6 mils thickness, and the second circuit's laminate is 20 mils thick. The laminate has a dielectric constant of 3.66, dissipation factor of 0.0037 and is commonly used in high-frequency applications.

It can be seen in Figure 1 that the table on the left for the thinner circuit has much lower radiation losses than the table on the right for the thicker circuit. It is also obvious that the radiation losses are frequency dependent and the higher frequencies have the higher radiation loss values.

The next example demonstrates the differences in radiation losses for circuits using the same thickness of matieral, but with different dielectric constants. Figure 2 shows a comparison of 50 ohm microstrip transmission lines using high-frequency laminates of 20 mil thickness, with a dielectric constant of 2.20 and 4.50.

50 ohm microstrip, Dk=2.20, Df=0.0009, thickness=20mil

Freq (GHz)	Dielectric Loss (dB/in)	Conductor Loss (dB/in)	Radiation Loss (dB/in)	Total Loss (dB/in)
1	-0.002	-0.016	0.000	-0.019
5	-0.012	-0.039	-0.014	-0.066
10	-0.024	-0.060	-0.056	-0.142
15	-0.037	-0.079	-0.127	-0.244
20	-0.050	-0.097	-0.225	-0.373
25	-0.063	-0.115	-0.350	-0.529
30	-0.077	-0.131	-0.502	-0.711

50 ohm microstrip, Dk=4.50, Df=0.002, thickness=20mil

Freq (GHz)	Dielectric Loss (dB/in)	Conductor Loss (dB/in)	Radiation Loss (dB/in)	Total Loss (dB/in)
1	-0.007	-0.036	0.000	-0.045
5	-0.038	-0.103	-0.010	-0.152
10	-0.078	-0.151	-0.042	-0.272
15	-0.118	-0.189	-0.095	-0.403
20	-0.160	-0.221	-0.168	-0.550
25	-0.203	-0.250	-0.261	-0.714
30	-0.247	-0.276	-0.373	-0.897

Figure 2: Comparison of losses for microstrip transmisison line circuits, with different dielectric constant, using the same substrate thickness.

MICROWAVE RADIATION LOSS CONCERNS IN PCBS *continues*

Figure 2 illustrates how a microstrip circuit with the same laminate thickness will have different radiation losses when using substrates with a different dielectric constant. The table on the left has much more radiation loss when using material with a dielectric constant of 2.20 than the table on the right with a circuit that features material with a dielectric constant of 4.50.

It can also be seen in Figure 2 that the dissipation factor (Df) is very different between these two materials. The Df mainly affects dielectric losses. The conductor losses are mostly dominated by copper properties, conductor width and surface roughness. Even though the material with a higher dielectric constant will have less radiation loss, it is necessary to have a narrower conductor width to maintain a 50 ohm trace, so the conductor losses will be higher than a circuit with a lower dictric constant. This is one of many tradeoffs that are to be expected when considering the proper material for an application.

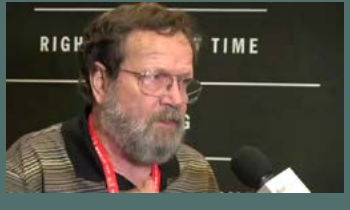
Radiation loss can be problematic for microwave PCB performance, however, it can also cause issues by radiating energy to neighboring conductors and components on the PCB. A thorough understanding of radiation loss can help to minizize EMI issues as well as optimizing the circuit for higher-frequency performance. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division. About half of his 25 years of professional experience has been spent in the flexible PCB industry doing circuit design, applications, processing, and materials engineering. Coonrod has also supported the high-frequency, rigid PCB materials made by Rogers for the past 10 years. Reach Coonrod here.

video interview

Lee Ritchey: Seeking the Limits of Materials

by Real Time with... PCBDesign007



At what speed will current materials fail? Lee Ritchey and Isola teamed up on this 16-layer test board that's designed to plumb the absolute limits of today's materials. Lee presented a well-attended paper on this subject at DesignCon 2013.

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Most-Read Mil/Aero007 News Highlights

FTG's New Facility Now Certified to AS9100C

FTG Aerospace - Chatsworth, a subsidiary of Firan Technology Group Corporation, has achieved certification to the ISO9001: 2008/AS9100 Revision C standard. FTG Aerospace - Chatsworth is the fifth FTG manufacturing facility to achieve AS9100 Revision C certification, demonstrating FTG's commitment to investing in its quality management systems.

Circuit-Tech Inc. Earns AS 9100C Certification

This AS9100C certification reflects the company's commitment to continuous improvements. Circuit-Tech Inc. also holds certificates for MIL-PRF 55110, ISO 9001-2000, and ISO 9001-2008, as well as the Canadian Controlled Goods Certificate.

Invotec Wins SC21 Bronze Award

Invotec Group's Tamworth facility has received the SC21 Bronze Award. To net this recognition, Invotec achieved delivery and quality performance standards for all of its key customers over a rolling 12-month period.

Lab Circuits Earns UNE-EN 9100:2010

Lab Circuits has been awarded the UNE-EN 9100:2010 certification for its Quality Management System, as required in the aviation, space, and defence sectors. In November, Lab Circuits successfully passed the certification audit for the quality standard UNE-EN 9100:2010 by AENOR.

China, India, Brazil Key Markets for Defense Growth

According to the survey results, 78%, 73%, and 56% of respondents from defense organizations identified 'cyber warfare,' 'UAVs,' and 'soldier modernization' as the most important defense segments that will show the most technological advancement over the next decade.

U.S. Defense Market Driven by Modernization

Research and Markets has announced the addition of the "Future of the U.S. Defense Industry - Market Attractiveness, Competitive Landscape and Forecasts to 2017" report to their offerings.

Technology Integration Vital to Ensure Enhanced Security

Constant threats related to terrorism and natural disasters are pushing city officials to build secure environments for residents. In order to ensure enhanced security that does not strain city budgets, optimization and integration of security technologies is imperative.

Global Military Comm & COTS Market at $17.46B in 2013

The Global Military Communications & COTS Market 2013-2023, Visiongain's latest defense and security report, values the market for military communications spending to reach $17.4B in 2013, as both mature and emerging national markets invest in advanced military communications networks.

Defense Industry to See Significant M&A Trend in 2013

The global defense industry witnessed significant M&A activity in 2012. The prevalent unstable economic environment and consequent federal military budget cuts in the major spending countries of North America and Europe resulted in consolidation as a primary growth strategy for companies.

Report Reveals Continued Decrease in Defense Sector Revenue & Earnings

Defense firms revenue decreased 1.5% and earnings fell 7.4%, while commercial aerospace revenue increased 18.3% and earnings increased by 13%.

The Ten Commandments of Design for Assembly

by Amit Bahl

SUMMARY: The best way for designers to avoid problems during assembly is to communicate thoroughly and frequently with your assembly provider. But, just in case, columnist Amit Bahl has created the Ten Commandments of DFA.

You might think that most PCB designers would know how to avoid the most obvious blunders that can gum up board assembly. But you would be wrong. I can tell you from daily experience that we're just not there yet. So allow me to propose the Ten Commandments of DFA.

1st Commandment

Be sure all indicators are present. The leading show-stopper in assembly is missing pin 1 indicators or component polarity/orientation indicators on the silkscreen. Nearly 75% of the assembly orders my facility receives fail to identify the location of pin 1 for each IC, or they misrepresent or neglect to indicate the polarity of some capacitors, diodes, or LEDs.

Obey the convention for marking the polarity of diodes, including LEDs: Put a K on the silkscreen layer at the cathode end. Alternatively, use the electrical symbol for diodes in the correct orientation to guide assembly. Never indicate diode polarity based on the anode pad. Use a K to designate the cathode or line up the diode symbol in the correct position. Don't substitute any other marks or your contractor will misinterpret what you intend.

To orient tantalum capacitors, tag the positive side with a plus symbol on the silkscreen. Remember, tantalum capacitors can ignite if mounted with swapped polarity. Short of reverse-engineering a schematic (and who bundles schematics with assembly files?) there's no way for a contractor to figure out part polarity unless it's clearly displayed.

Silkscreens must not interfere with pads, and symbols should not be printed beneath the body of any component.

2nd Commandment

Vias in pads must be filled, unless they reside in thermal pads. The pad matrix on which a BGA will be installed may include through vias and blind vias, but all of them must be filled and planarized, or solder joints will be compromised.

Incorporate vias in the thermal pads under QFNs to help solder flow through to conductive planes. The vias ensure a secure solder joint for the thermal pad and prevent solder from floating the

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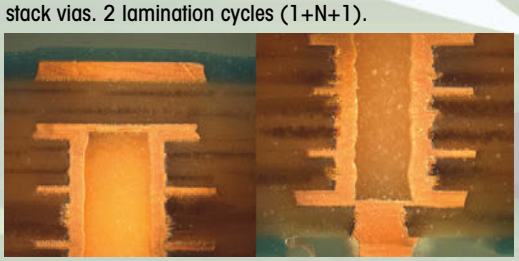
Example Test Vehicle

18 layer, .085" thick (2.16 mm), buried and single stack vias. 2 lamination cycles (1+N+1).



(Magnified @ 100x)

Results include:

- 10x reflow @ 260°C (JEDEC std. lead free cycle) ,
- 6x 260°C preconditioning before 1000 cycles IST @ 150°C followed by 100 cycles @ 190°C
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THE TEN COMMANDMENTS OF DESIGN FOR ASSEMBLY *continues*

package during assembly, which could hamper forming good solder joints at the QFN contacts. An assembly shop can compensate for a lack of through vias in a thermal pad by adding a windowpane-shaped opening in the solderpaste stencil above the pad, to relieve solder pooling and outgassing during assembly, but the fix is less effective than if vias were present.

3rd Commandment

Every connection to every component must have its own independent pad. Each pad must be commensurate in size with its mates.

If two components share a pad – let's say, a resistor and a capacitor – neither can be properly aligned during assembly. And if one pad is substantially larger than its mate for a component, component tombstoning can result from an imbalance of solder deposition.

If a pour or plane will be a point of contact, there must be a mask-defined pad of appropriate size. If a device involves non-soldermask-defined pads for connections as well as soldermask-defined pads – a BGA matrix on a loose pitch in which some adjacent outer balls are common to a ground pour, for example – stipulate in a design note that the board fabricator shall not edit the soldermask apertures for those soldermask-defined pads.

4th Commandment

Never mix lead-free components with components that are not specified for lead-free assembly. If any component requires lead-free assembly and no substitute for conventional leaded solder is available, then the entire board must be assembled lead-free and all components must be qualified for lead-free assembly.

Sometimes the only package available for a particular device is a lead-free BGA. However, boards that will be used for military projects

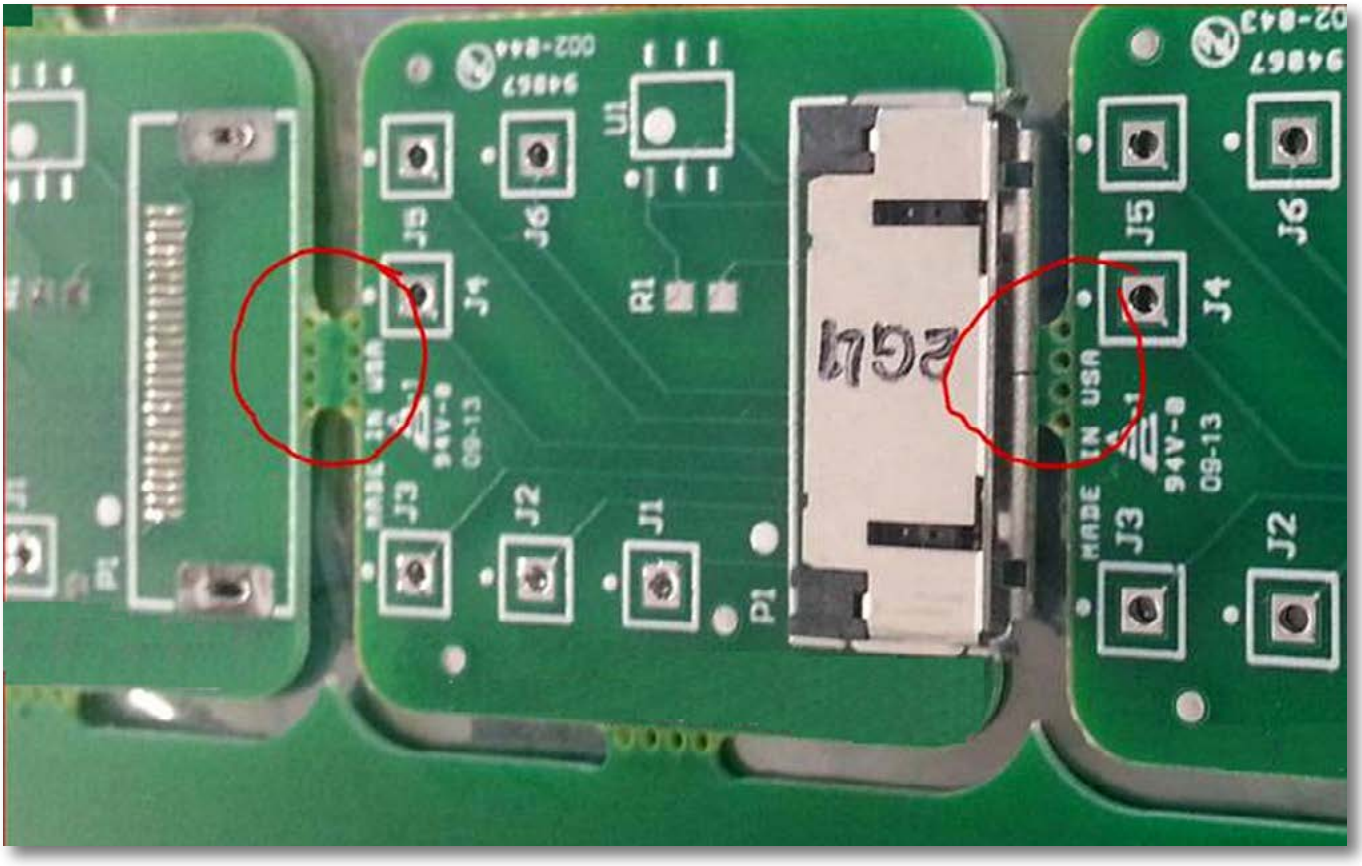

Figure 1: A breakaway tab that remained between these boards after routing interfered with assembling a connector that extends over that edge. Such problems occur when board fabrication and assembly are not closely coordinated.

typically must be assembled with conventional leaded solder, per government requirements. The designer must either obtain a waiver from the customer to allow lead-free assembly; modify the design to use a device that is available in a package for assembly with conventional leaded solder; or have the BGA reballed for leaded solder (an expensive procedure that can damage parts).

5th Commandment

Adhere to spacing guidelines, including clearances at board edges. If connectors or other hardware will overlap a board edge, and the boards will be fabricated by one vendor and assembled by another, instruct the fabricator where the connectors will sit and to route panels such that no material remains that would interfere with the connectors during assembly (Figure 1).

6th Commandment

Distribute large components across a board as evenly as possible during layout, to achieve the best possible thermal distribution during solder reflow. Make sure the assembly contractor tailors a thermal profile for the reflow oven unique to each assembly job.

7th Commandment

Format every bill of materials according to Figure 2, to precisely identify all of the components to be assembled on each board. The properly formatted BOM has columns indicating:

- full manufacturer's part number
- manufacturer's name
- item number
- quantity per board
- reference designators, separated by commas
- a complete part description

It may also include:

- distributor's name
- distributor's part number

8th Commandment

Boards should be provided as arrays in panels for assembly if they are very small, especially those smaller than 3" x 3". All irregularly shaped boards (circular, oval, L-shaped, etc.) should be arrayed to facilitate handling. Some contractors can assemble a limited number of such small or odd-shaped boards individually, using universal fixtures.

Follow these guidelines:

- One BOM for the entire panel. For example, if there are four different boards called A, B, C, D, a single BOM must list all of the components for all four boards combined.
- None of the reference designators can be repeated from one board to another. For example, if R1 will be assembled on board A, it cannot be used as a designator on any of the other boards. If a part of the same value is required on other boards, it must be designated differently for each board.

Part Number	Item	qty	Designator	Description	Mank
C2012X5R1C106K/1.25	1	1	C1	CAP CER 10UF 16V 10% X5R 0805	TDK
C2012X5R0J476M	2	1	C2	CAP CER 47UF 6.3V X5R 20% 0805	TDK
C1608X7R1A105K	3	5	C3, C132, C133, C136, C137	CAP CERAMIC 1.0UF 10V 0.1 X7R 0603	TDK
C2012X5R1A226K/1.25	4	4	C4, C16, C19, C24	CAP CER 22UF 10V 10% X5R 0805	TDK
C1005X5R0J104K	5	15	C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C20, C118, C119, C120	CAP CERAMIC .10UF 6.3V 0.1 X5R 0402	TDK

Figure 2: Prepare the BOM for every project in exactly the same format. Adhere to this example.

THE TEN COMMANDMENTS OF DESIGN FOR ASSEMBLY *continues*

Figure 3: A proper kit would contain one contiguous tape of this component, including overage.

• Placement must be guided by a single set of XY data for the entire panel in correlation with the single, combined BOM.

9th Commandment

Needless to say, it's far better to catch issues that might impede assembly before the boards are fabricated. If the board will be fabricated and assembled by the same facility (thereby coordinating operations), verify whether to provide the design data in ODB++ format to speed identifying potential manufacturing issues and ease CAM setup. Outputting a design in ODB++ captures the data for fabrication, assembly, and test in a unified structure that supports automated analysis and avoids time-consuming data conversion at the CAM stage. Practically all major EDA platforms can output design data in the ODB++ format.

10th Commandment

Technically, the 10th commandment does not address design, but component delivery to the contractor. If assembly will be performed on a consignment basis – some or all of the components will be supplied by the assembly customer, instead of being procured by the assembler – the parts must be provided in a carefully organized kit matching the BOM. All SMT components must be supplied in reels, or on continuous tapes at least 6" in length, or in tubes or trays.

Extra components are required for every part number listed on the BOM, to cover attrition during assembly. For example, an assembly shop may require a minimum of 100, or 20% more 0201 1k ohm resistors than called for on the BOM. The parts for each line item on the BOM must be sent in a clearly marked bag separate from the other parts. All ICs must be shipped in their original, unopened protective packages that include desiccant, or else they must be baked for eight hours or so to remove moisture before assembly, which could set back assembly for a day.

In other words, eight strips of eight pieces of a 1005-size 12-pF capacitor do not fulfill a BOM requirement for 64 pieces of that part. The strips are too short for loading the pick-and-place feeders, and under the best circumstances not all the parts will wind up on boards (Figure 3).

Let me conclude by recommending the best way to avoid assembly problems: Confer with your manufacturer before design even begins. **PCBDESIGN**

Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached by clicking here.

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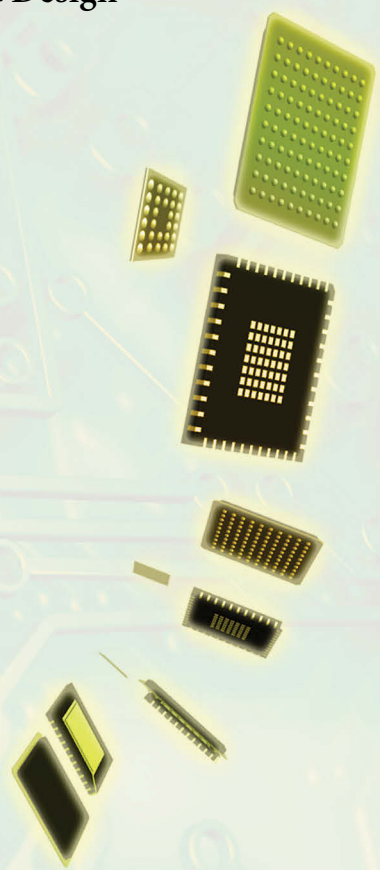

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Top 10 Key EMC Design Considerations

by Ashish Kumar and Pushek Madaan
CYPRESS SEMICONDUCTOR

SUMMARY: ***For years, PCB designers didn't worry too much about EMC issues. But now, designers are realizing that proper design techniques can indeed help to eliminate EMI. Ashish Kumar and Pushek Madaan of Cypress Semiconductor have crafted a handy Top 10 list of EMC design tips.***

Any electronic product consists of various modules, where each module has to communicate with the other for its operation or to report the status. With the ever-growing demand for faster processing speeds, better response time and more throughputs, always narrow down to high-speed circuits. If not contained properly, the signal flowing through these circuits may radiate energy and can cause problems in the operation of devices in the near vicinity.

Now, engineers must consider not only the actual logic on the PCB, but also several other aspects that affect the circuit, including power consumption, PCB size, environment noise, and EMC. The following 10 key EMC design considerations can serve as guidelines and describe how hardware engineers can address EMC issues during the PCB design phase for a system free of EMC faults:

1. Ground Planes: A low-inductance ground system is the most vital element when designing a PCB for minimizing EMI. Maximizing the ground area on a PCB reduces the inductance of ground in the system, which in turn reduces electromagnetic emissions and crosstalk.

Signals can be connected to ground using different methods. In a poor PCB design, components are connected randomly to ground points. Such a design generates high ground inductance and leads to unavoidable EMC issues.

A recommended design approach is to utilize a full ground plane, because it provides the lowest impedance as the current returns back to its source. However, a ground plane requires a dedicated PCB layer which may not be feasible for two-layer PCBs. In such cases, designers should use ground grids, as shown in Figure 1a. The inductance of ground in this case will depend on the spacing between the grids.

The way a signal re-

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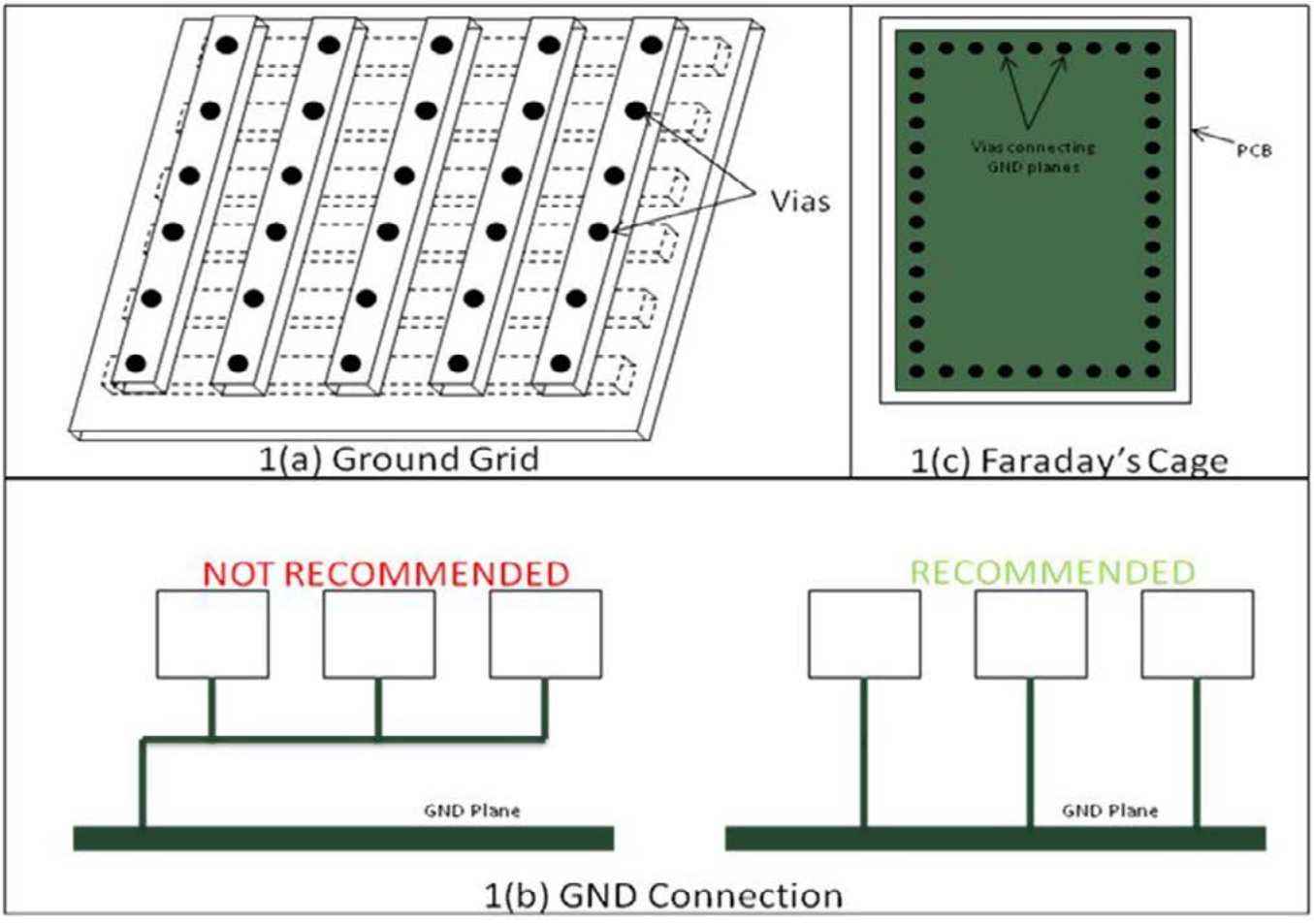

Figure 1: EMC design techniques: 1(a) depicts the recommended ground grid. 1(b) shows recommended and not recommended ground connections. 1(c) details a Faraday cage.

turns to system ground is also very important because when a signal takes a longer path, it creates a ground loop, which forms an antenna and radiates energy. Thus, every trace carrying current back to the source should follow the shortest path and must go directly to the ground plane. Connecting all the individual grounds and then connecting them to the ground plane is not advisable because it not only increases the size of current loop but also increases the probability of ground bounce. Figure 1b shows the recommended method of connecting components to the ground plane.

A Faraday cage is another good mechanism for reducing EMI. A Faraday cage is formed by stitching the ground on the complete periphery of the PCB and not routing any signal outside this boundary (see Figure 1c). This mechanism restricts the emission/interference from/to the PCB within/outside the boundary defined by the cage.

2. Component Segregation: For an EMI-free design, components need to be grouped on the PCB according to their functionality, such as analog, digital, power supply sections, low-speed circuits, high-speed circuits, and so on. The tracks for each group should stay in their designated area. For a signal to flow from one subsystem to another, a filter should be used at subsystem boundaries.

3. Board Layers: From an EMC point of view, proper arrangement of the layers is vital. If more than two layers are used, then one complete layer should be used as a ground plane. In the case of a four-layer board, the layer below the

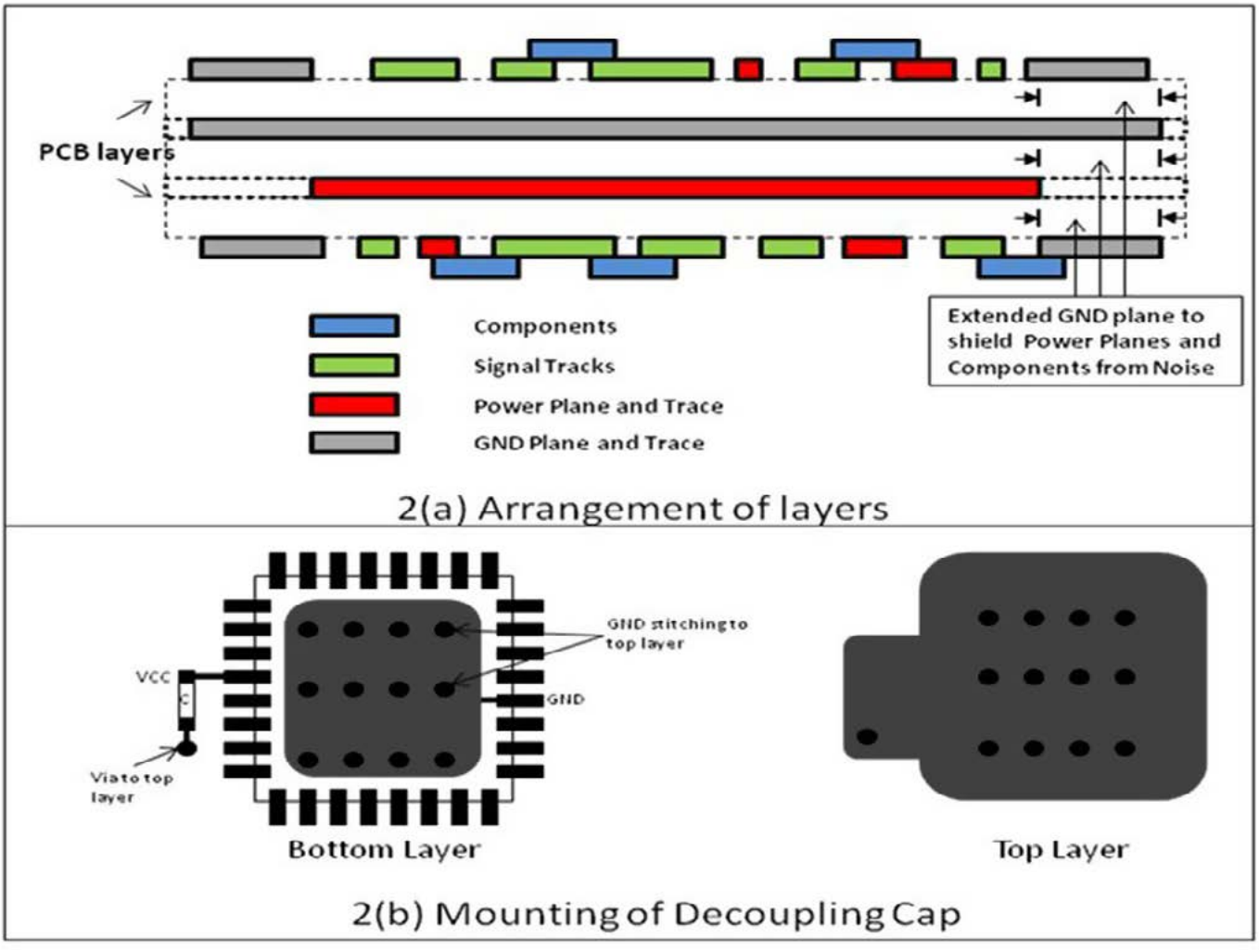

Figure 2: 2(a) shows an optimum arrangement of PCB layers for EMC. 2(b) depicts the correct mounting of a decoupling capacitor.

ground layer should be used as a power plane (Figure 2a shows one such arrangement). Care must be taken that the ground layer is always between high-frequency signal traces and the power plane. If a two-layer board is used and a complete layer of ground is not possible, then ground grids should be used. If a separate power plane is not used, then ground traces should run in parallel with power traces to keep the supply clean.

4. Digital Circuits: When dealing with digital circuits, extra attention must be given to clocks and other high-speed signals. Traces connecting these signals should be kept as short as possible and be adjacent to the ground plane to keep radiation and crosstalk under control. With such signals, engineers should avoid using vias or routing traces on the PCB edge or near connectors. These signals must also be kept away from the power plane since they are capable of inducing noise on the power plane as well.

While routing traces for an oscillator, apart from ground no other trace should run in parallel or below the oscillator or its traces. The crystal should also be kept close to the appropriate chips.

It is also worth noting that return current always follows the least reactance path. Therefore, ground traces carrying return current should be kept close to the trace carrying its associated signal to keep the current loop as short as possible.

Traces carrying differential signals should

run close to each other to most effectively use the advantage of magnetic field cancellation.

5. Clock Termination: Traces carrying clock signals from a source to a device must have matching terminations, because whenever there is an impedance mismatch, a part of the signal gets reflected. If proper care is not provided to handle this reflected signal, large amounts of energy will be radiated. There are multiple forms of effective termination, including source termination, end termination, AC termination, etc.

6. Analog Circuits: Traces carrying analog signals should be kept away from high-speed or switching signals and must always be guarded with a ground signal. A low-pass filter should always be used to get rid of high-frequency noise coupled from surrounding analog traces. In addition, it is important that the ground plane of analog and digital subsystems not be shared.

7. Decoupling Capacitors: Any noise on the power supply tends to alter the functionality of a device under operation. Generally, noise coupled on the power supply is of a high frequency, thus a bypass capacitor or decoupling capacitor is required to filter out this noise. A decoupling capacitor provides a low-impedance path for high-frequency current on the power plane to ground. The path followed by the current as it travels toward ground forms a ground loop. This path should be kept to a minimum level by placing a decoupling capacitor very close to the IC (Figure 2b). A large ground loop increases the radiation and can act as a potential source of EMC failure.

The reactance of an ideal capacitor approaches zero with increasing frequency. However, there is no such thing as an ideal capacitor available on the market. In addition, the lead and the IC package add inductance as well. Multiple capacitors with low ESL (equivalent series inductance) should be used to improve the decoupling effect.

8. Cables: Most EMC-related problems are caused by cables carrying digital signals that effectively act as an efficient antenna. Ideally, the current entering a cable leaves it at the other end. In reality, parasitic capacitance and inductance emit radiation. Using a twisted pair cable helps keep coupling to a low level by cancelling any induced magnetic fields. When a ribbon cable is used, multiple ground return paths must be provided. For high-frequency signals, shielded cable must be used where the shielding is connected to ground both at the beginning and at the end of the cable.

9. Crosstalk: Crosstalk can exist between any two traces on a PCB. It is a function of mutual inductance and mutual capacitance proportional to the distance between the two traces, the edge rate, and the impedance of the traces. In digital systems, crosstalk caused by mutual inductance is typically larger than the crosstalk caused by mutual capacitance. Mutual inductance can be reduced by increasing the spacing between the two traces or by reducing the distance from the ground plane.

10. Shielding: Shielding is not an electrical solution but a mechanical approach to reducing EMI. Metallic packages (conductive and/or magnetic materials) are used to prevent emissions from escaping the system. A shield may be used either to cover the whole system or a part of it, depending upon the requirements. A shield is like a closed conductive container connected to ground, which effectively reduces the size of loop antennas by absorbing and reflecting a part of their radiation. In this way, a shield also acts as a partition between two regions of space by attenuating the radiated EM energy from one region to another. A shield reduces the EMI by attenuating both the E-field and H-field component of radiating wave. **PCBDESIGN**

Ashish Kumar is a senior product engineer with Cypress Semiconductor.

Pushek Madaan is a senior application engineer with Cypress Semiconductor.

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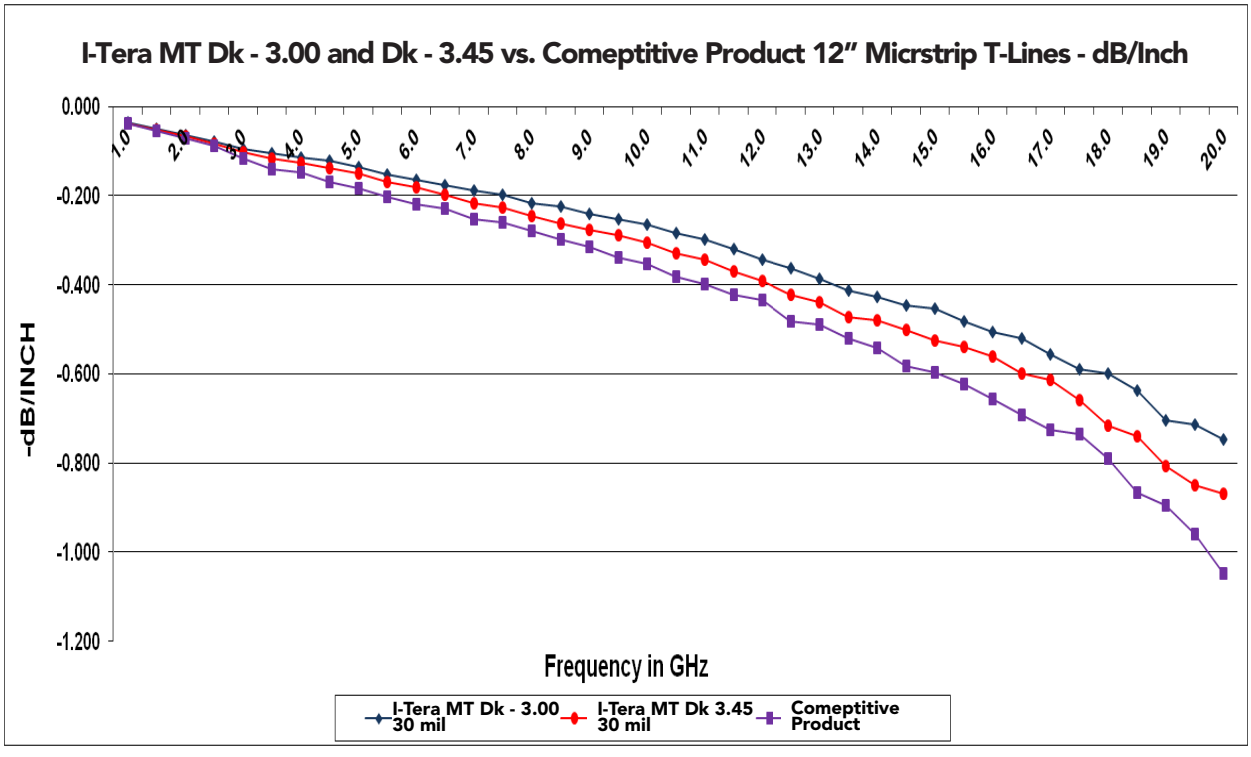

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DesignCon: The Early Years

by Istvan Novak

SUMMARY: ***It's been almost 20 years since Istvan Novak first attended the Hewlett Packard conference that eventually became DesignCon. Much of the technology has changed in the past two decades, but the Silicon Valley staple has primarily remained true to its roots.***

DesignCon, held in late January or early February each year in Santa Clara, California, attracts signal and power integrity practitioners from around the globe[1]. Anyone who only recently began attending this conference may not be aware that, even though DesignCon's history is not as long as some other professional conferences (such as those sponsored by IEEE), DesignCon got its start about 25 years ago.

My first experience with what later became DesignCon occurred almost exactly 20 years ago. On April 5, 1993, in Budapest, Hungary, I attended a High-Speed Digital Design Symposium.

For readers in the younger generation, it is worth mentioning that Hewlett Packard in those years was known mostly for measurement solutions provided by the business unit that later became Agilent. There were two tracks

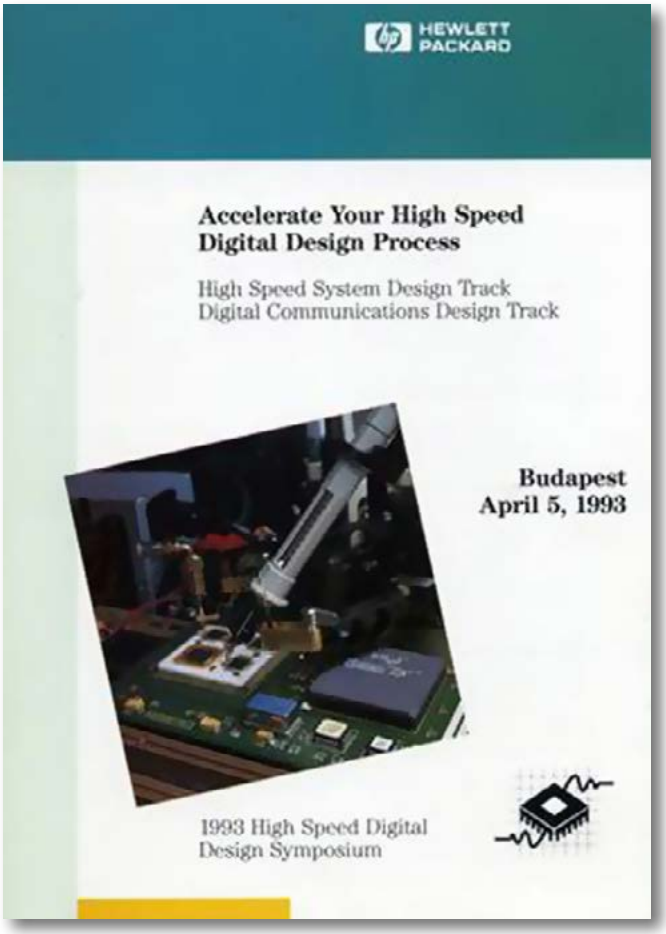

Figure 1: Front page of the conference flyer for the April 5, 1993 High Speed Digital Design Symposium, sponsored by Hewlett Packard.

Technical Presentations

Concepts discussed in the presentations will be demonstrated in the Exhibit Room throughout the day. Speakers will participate in these demonstrations, and you are invited to join them for informal discussions.

Track A
High Speed System Design

1. Michael K. Williams: Amherst Systems Associates
Distortion and Tolerance Mechanisms and High-Speed Clock Delivery
The steady increase in system complexity and performance goals make the precise delivery of the system clock edge an important design issue. In this paper we examine the primary sources of clock skew and jitter that degrade precise clock edge delivery.

2. Eric Blomberg: Hewlett-Packard Apollo
Glitches, Intermittents and Noise Problems ... The Art of Noise-Budgeting
What are the major causes of intermittent failure in digital designs? What is the origin of these effects and what can be done to minimize them? We discuss these issues and more, including tips on building-in reliability through noise budgeting. Case studies are used throughout.

3. Henri Merkelo: University of Illinois
Advanced Methods for Noise Cancellation in System Packaging
Digital signals can be degraded by packaging effects such as reflection noise, crosstalk noise, and simultaneous switching noise. This paper analysis resistive and reactive matching, with design criteria developed based on the degree of desired compensation and noise suppression. Using case studies of vias, bends, and interposer contacts, we provide guidelines for reactive noise cancellation, and verification of designs using CAE simulation tools.

4. Michael L. Conn: Mikon Consulting
Printed Circuit Design Techniques for the Control of Electromagnetic Interference
Differential-mode (DM) and common-mode (CM) radiation interference are a major problem in the design of printed circuit boards (PCBs) intended for use in high-speed circuit designs. Using the comparative characteristic performance and performance of microstrip and stripline construction techniques, we present methods of predicting, avoiding, suppressing and containing radiated emissions created by modern high-speed circuits. We identify and discuss the roles of CAE design tools and test and measurement equipment.

5. Pat Byrne and Greg Walz: Hewlett-Packard R&D
Debugging and Characterising Ground Bounce Problems in High-Speed Memory System Hardware
When bus width, speed and physical densities are improved, new hardware failure mechanisms begin to plague a design. This paper describes a case study in debugging and characterising a multiple-bus memory system. We explain the physical mechanism of ground bounce and apply it to design techniques that improve the performance and operating reliability of high-speed memory bus designs.

6. Ken Smith: Cascade Microtech
Feasibility of Moving a 50MHz Design to Run at 100MHz
Using a 50-MHz, 486-cache as a design example, we address the problem of doubling the speed to 100 MHz. The process used involves measurement, modelling, and simulation techniques. Substrate measurements are used to show which transmission line models are appropriate. Using fine-pitch probing methods, we show how to verify critical signals against simulations.

Figure 2: The papers, presenters and abstracts of Track A, High Speed Digital Design.

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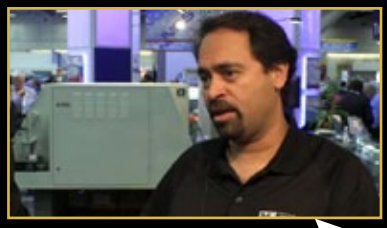

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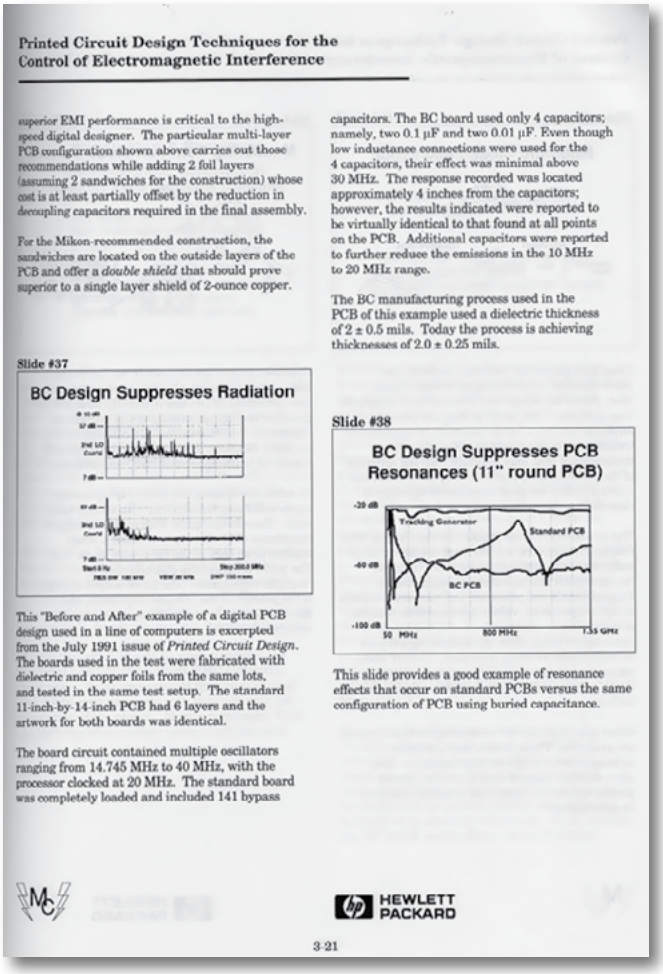
DESIGNCON: THE EARLY YEARS *continues*

in the symposium: High Speed System Design and Digital Communications Design. Figure 2 shows.

Each paper presentation was an hour session, and the day concluded with demonstrations by the presenters in the spacious hallway. Among others, I remember Michael Williams demonstrating the clock jitter and skew with his custom-built circuit, the demonstration with fine-pitch probes measuring the signals on a multichip module (also shown in Figure 1), and the close-field probe measurements of PCB radiation by Michael Conn and Henri Merkelo demonstrating the compensation options of via discontinuities.

The big news in those days: Is it possible to run a system at 100 MHz clock speed that was designed for 50 MHz? Most papers focused on signal integrity, though in those years even the term signal integrity was not widely used yet. Power integrity had no dedicated paper at this conference, but if we read the papers carefully, we can find several related topics that later became important pieces of power integrity. For instance, Michael Conn's paper, "Printed Circuit Design Techniques for the Control of Electromagnetic Interference," devoted three pages and five slides to the buried capacitance concept from Zycon Corporation. The third of these pages is reproduced in Figure 3. In case you are interested in reading the full paper but cannot find it, read on: It will become available.



Printed Circuit Design Techniques for the Control of Electromagnetic Interference

superior EMI performance is critical to the high-speed digital designer. The particular multi-layer PCB configuration shown above carries out those recommendations while adding 2 foil layers (assuming 2 sandwiches for the construction) whose cost is at least partially offset by the reduction in decoupling capacitors required in the final assembly.

For the Mikon-recommended construction, the sandwiches are located on the outside layers of the PCB and offer a *double shield* that should prove superior to a single layer shield of 2-ounce copper.

capacitors. The BC board used only 4 capacitors; namely, two 0.1 μF and two 0.01 μF. Even though low inductance connections were used for the 4 capacitors, their effect was minimal above 30 MHz. The response recorded was located approximately 4 inches from the capacitors; however, the results indicated were reported to be virtually identical to that found at all points on the PCB. Additional capacitors were reported to further reduce the emissions in the 10 MHz to 20 MHz range.

The BC manufacturing process used in the PCB of this example used a dielectric thickness of 2 ± 0.5 mils. Today the process is achieving thicknesses of 2.0 ± 0.25 mils.

Slide #37

BC Design Suppresses Radiation

This "Before and After" example of a digital PCB design used in a line of computers is excerpted from the July 1991 issue of *Printed Circuit Design*. The boards used in the test were fabricated with dielectric and copper foils from the same lots, and tested in the same test setup. The standard 11-inch-by-14-inch PCB had 6 layers and the artwork for both boards was identical.

The board circuit contained multiple oscillators ranging from 14.745 MHz to 40 MHz, with the processor clocked at 20 MHz. The standard board was completely loaded and included 141 bypass

Slide #38

BC Design Suppresses PCB Resonances (11" round PCB)

Tracking Generator
Standard PCB
BC PCB
-20 dB
-60 dB
-100 dB
50 MHz
800 MHz
1.55 GHz

This slide provides a good example of resonance effects that occur on standard PCBs versus the same configuration of PCB using buried capacitance.

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3-21

Figure 3: Page 21 of Michael Conn's paper describing the benefits of 2-mil laminates.

When I tried to locate proceedings of this conference from earlier years, I came up empty. Unfortunately, these conference proceedings did not have an ISBN number, and to confuse things further, there were also other events with similar names. Based on the proceedings I have found from 1993, I tried to find at least some of those papers online. It turns out that there are a few websites dedicated to preserving the technical history of Hewlett Packard. One is www.hparchive.com[2], a site maintained by Glenn Robb. Under the HP Seminars header, I found one (and only one) scanned paper from the US version of this High Speed Digital Design Symposium. I asked my friends and colleagues, who had more direct information about the early years of this conference series. Karl Kachigan of Agilent offered a brief summary of his first-hand experience. Karl was part of the team that created Design SuperCon, and offered his perspective.

Karl wrote in an e-mail:

A group in the Americas created the first High Speed Digital Seminar in 1989. It was given in the HP Santa Clara office by HP marketing folks. For the next few years, 1990-1992, that seminar evolved using some consultants to create and deliver some presentations, and was delivered at several cities in the US. In 1993, we again ran the seminar tour and first did one in Europe. In 1994, seminar tours focused on ATM/broadband and communications. To simplify equipment setup, we created custom carts that could be wheeled into the hotels and back onto a big 18-wheel moving van. The carts stored the equipment beneath,

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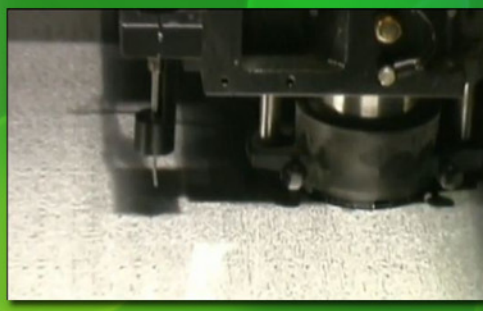

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DESIGNCON: THE EARLY YEARS *continues*

and showcased it on top. There were custom back boards with signage. I remember having to wheel these things around.

At that point, it was getting difficult to coordinate the consultants, equipment, and travel to multiple cities. We had enlisted a moving company to get stuff from city to city, so just getting schedules setup was a challenge. We determined that it would be better to hold a symposium in one city over a few days instead of a seminar tour in eight cities.

The concept of the HP Design SuperCon was to solicit paper topics from consultants, provide some funding to those that looked best, and have them create a paper and associated demo of HP gear (actually, we used this process for the seminar tours in 1990 and on). The demos were in another area in a trade show format with the movable carts. We aggregated topics into 3 or 4 tracks – typically high speed design, system design, package design, and ASIC/IC design. In 1995, we held the first HP DesignSuperCon at the Santa Clara Marriott. We had a big tent outside for registration, used a large room for the tradeshow, and several other rooms a bit of a walk away for the papers. Books were printed for each of the tracks. I have one from the system design track. I left many others with someone in EEsof when I left the group. The papers were never available in electronic form, not even PDFs, so if you found anything, it was likely a scan of the pages from the book. I found the 1995 call for papers, which provides some interesting insight into that first Design SuperCon.

We branched out and held the event in the U.S. and Japan for the next few years. We had easily outgrown the Marriott and looked for another venue, which was the Santa Clara Convention Center. We started there in 1996, and targeted the last week of January for the show each year. In 1998, I think we dropped the "Super" from the name and it was then just called DesignCon.

In 2000, when the Internet bubble burst and HP had to cut expenses, we worked with the IEC, which acquired DesignCon. They drove the key decisions, solicited people to join the technical review committee, and expanded it from an HP-only event to an open event. HP/Agilent continued to be active in many aspects of the show and paid appropriate sponsor fees. I was involved with DesignCon again from 2003 to 2010 as the Agilent liaison. In 2003, we created an Executive Forum aimed at discussing the challenges managers experienced. In 2004, it evolved into a management track, which was quickly embraced by the EDA companies. In 2003, a DesignCon East was started in the Boston area, attempting to appeal to those on the East Coast. Unfortunately, it never had high attendance and the last event happened in 2005. In 2004, a Euro DesignCon appeared but the costs were high and I think it happened only once.

To this day, DesignCon has been fairly true to its roots, offering papers created by experts to train others on leading-edge topics with a tradeshow that is fairly tame compared with the big shows like DAC, MTT, etc.

To this day, DesignCon has been fairly true to its roots, offering papers created by experts to train others on leading-edge topics with a tradeshow that is fairly tame compared with the big shows like DAC, MTT, etc.

Now, DesignCon is managed by UBM and the DesignCon East events restarted a few years ago[4]. Unfortunately, as Karl confirmed, there is little chance to find the conference proceedings in a public library, but thanks to websites like www.hparchive.com, scanned papers from these conferences will be made available if people who have their own copies of the conference proceedings are willing to scan them and send the files to Glenn Robb. In the coming weeks I am going to scan the proceedings from 1993; you can now read the first scanned item[5].

If you are interested in the recent activities around DesignCon, you can follow the DesignCon Community website (www.designconcommunity.com)[6]. **PCBDESIGN**

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1. www.designcon.com
2. www.hparchive.com/
3. Proceedings for sonet case study at the 1993 High Speed Digital Design Symposium
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5. Proceedings for clock speed feasibility study at 1993 High Speed Digital Systems Design & Test Symposium
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Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To contact Istvan, click here.

DARPA Achieves Record Power Output

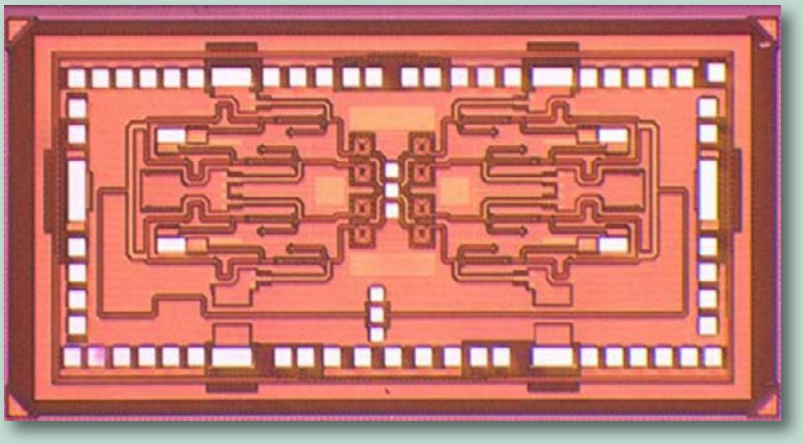
Two teams of DARPA performers have achieved world record power output levels using silicon-based technologies for millimeter-wave power amplifiers. RF power amplifiers are used in communications and sensor systems to boost power levels for reliable transmission of signals over the distance required by the given application. These breakthroughs were achieved under the Efficient Linearized All-Silicon Transmitter ICs (ELASTx) program.

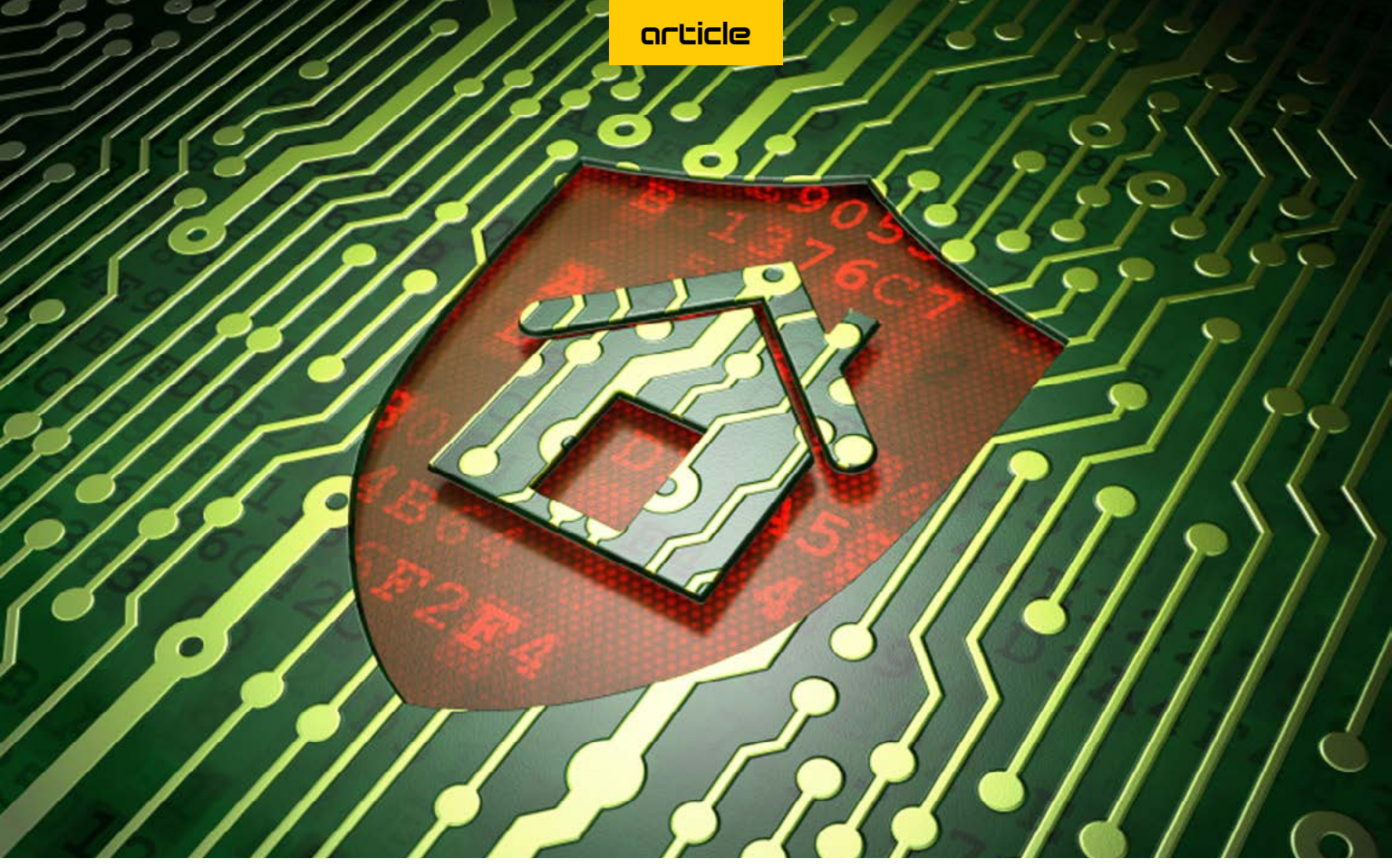
The first team, composed of performers at the University of Southern California and Columbia University, achieved output power levels of nearly 0.5 W at 45 gigahertz with a 45 nanometer silicon complementary metal oxide semiconductor (CMOS) chip. The chip design used multiple stacked 45 nanometer silicon-on-insulator CMOS devices for increased effective output voltage swing and efficient 8-way on-chip power-combining. Results will be reported at the 2013 Institute of Electrical and Electronics Engineers Radio Frequency Integrated Circuits Symposium.

The second team, made up of MIT and Carnegie Mellon University researchers, demonstrated a 0.13 micrometer silicon-germanium (SiGe) BiCMOS power amplifier employing multistage power amplifier cells and efficient 16-way on-chip power-combining. This amplifier has achieved power output of 0.7 W at 42 gigahertz, a 3.5 times increase in output power compared to the next best reported silicon-based millimeter-wave power amplifier; this result was reported at the 2013 International Solid-State Circuits Conference (ISSCC).

"Millimeter-wave power amplifiers have been demonstrated at this power level before, but this is a record with silicon-based technologies," said Sanjay Raman, DARPA program manager. "Producing this level of output with silicon may allow integration on a chip with complex analog and digital signal processing. In the 42-25 GHz range, this would enable high bandwidth/data-rate transmitters needed for satellite communications at potentially very low cost and size, weight and power."

Silicon-based circuit techniques developed under the ELASTx program may eventually be applied to even higher performance compound semiconductor devices, such as gallium nitride high electron mobility transistors.





Are Guard Traces Worth It?

by Bert Simonovich
LAMSIM ENTERPRISES

SUMMARY: ***Some claim that a guard trace should be shorted to ground at regular intervals along its length using stitching vias spaced at 1/10th of a wavelength of the highest frequency component of the aggressor's signal. But others believe separating the victim trace to at least three times the line width from the aggressor is good enough. Bert Simonovich addresses both arguments.***

By definition, a guard trace is a trace routed coplanar between an aggressor line and a victim line. There has always been an argument about whether to use guard traces in high-speed digital and mixed signal applications to reduce the noise coupled from an aggressor transmission line to a victim transmission line.

On one side of the debate, the argument is that the guard trace should be shorted to ground at regular intervals along its length using stitching vias spaced at 1/10 of a wavelength of the highest frequency component of the aggressor's signal. By doing so, it is believed the guard trace will act as a shield between the aggressor and victim traces.

On the other side, merely separating the victim trace to at least three times the line width from the aggressor is good enough. The reasoning is that crosstalk falls off rapidly with increased spacing anyway, and by adding a guard trace, you will already have at least three times the trace separation to fit it in.

In a DesignCon2013 paper that I coauthored along with Eric Bogatin, "Dramatic Noise Reduction using Guard Traces with Optimized Shorting Vias," we showed that sometimes, guard traces were effective, and sometimes they were not, depending on how the guard trace was terminated. By correct management of the ends of the guard trace, we demonstrated it can reduce coupled noise on a victim line by an order of magnitude over not having the guard trace present. But if the guard trace was not optimized, the noise on the victim line can also be larger with the guard trace, than without.

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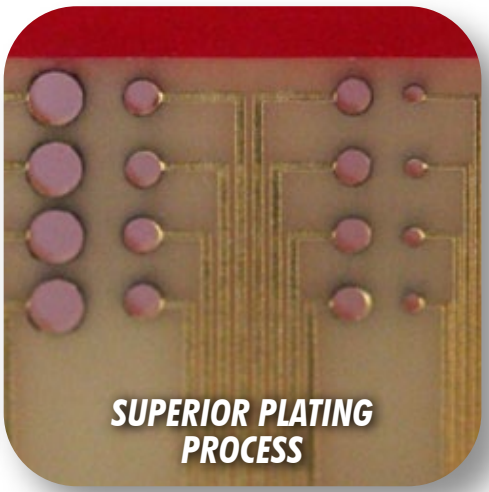

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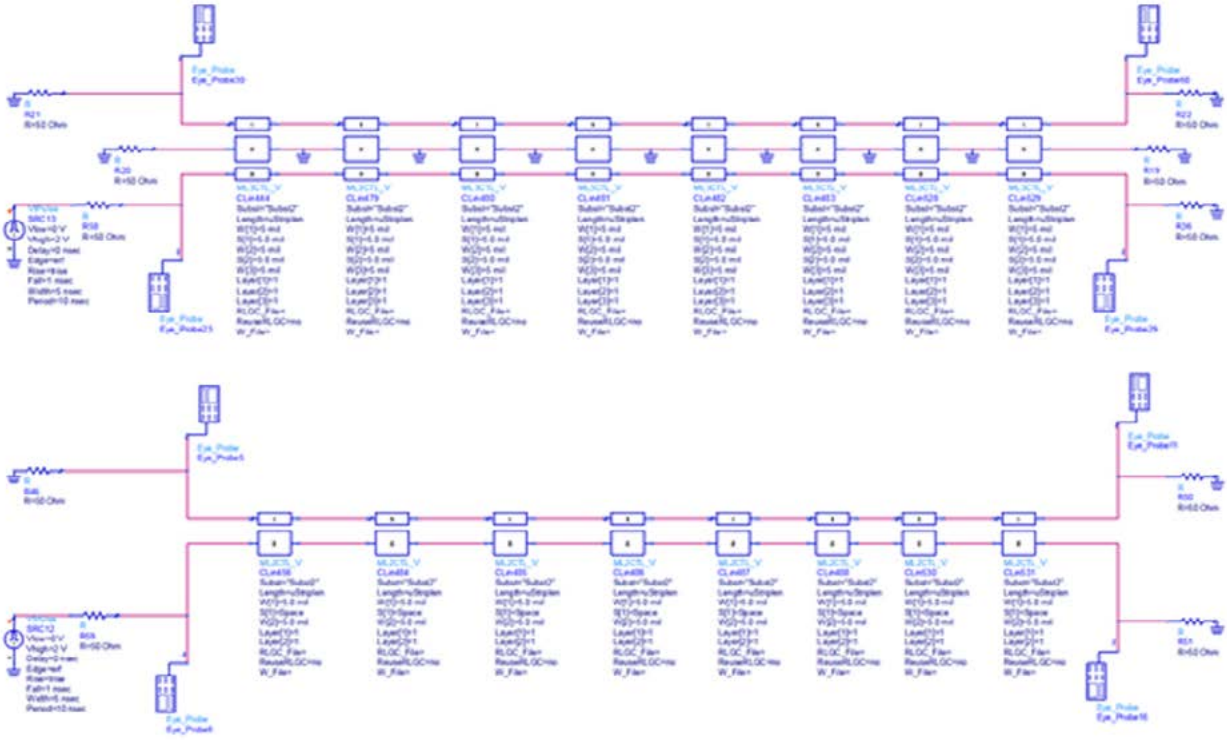

Figure 1: ADS schematic for generic topologies with a guard trace (top) and without (bottom). The transmission line were segmented and parameterized to easily change the lengths as required. The ground stitching and the end-termination resistors, shown in top schematic, can be deactivated and/or shorted as required.

Analysis Using Circuit Models

We started out the investigation by building circuit models for the topologies studied. Agilent's EEsof EDS ADS software was used exclusively to model and simulate both stripline and microstrip configurations. The generic circuit model, with a guard trace, is shown in the top half of Figure 1. The circuit model, without a guard trace, is shown in the bottom half.

For the analysis, we used lossless transmission line models. The guard trace length was exactly matched to the coupled length. The ground stitching and the end-termination resistors, on the guard trace, could be deactivated, and/or shorted, as required. The line-width space geometry was set at 5-5-5 mils, and the spacing for the non-guarded topologies was set to three times the line width.

Figure 2 is a summary of results when a guard trace was terminated in the characteristic impedance, left open, or shorted to ground at each end. The red waveforms are the results for topologies without a guard trace, and the blue waveforms are with a guard trace.

Depending on the nature of the termination, the reinfected noise on the guard trace can add to or subtract from the directly coupled noise on the victim line. This often makes the net noise on the victim line worse than without a guard trace.

Unlike a simple two-line coupled model, where the near-end crosstalk (NEXT) and far-end crosstalk (FEXT) can be easily predicted from the RLGC matrix elements, trying to predict the same for a three-line coupled model is more difficult. Manually keeping track of all the noise induced on the guard trace, and its reinfection onto the victim line, is extremely tedious. First you must identify the directly coupled reinfected backward and forward noise on the victim line from the voltage on the guard trace. Then the problem is keeping track of the multiple reflections of the noise on the guard

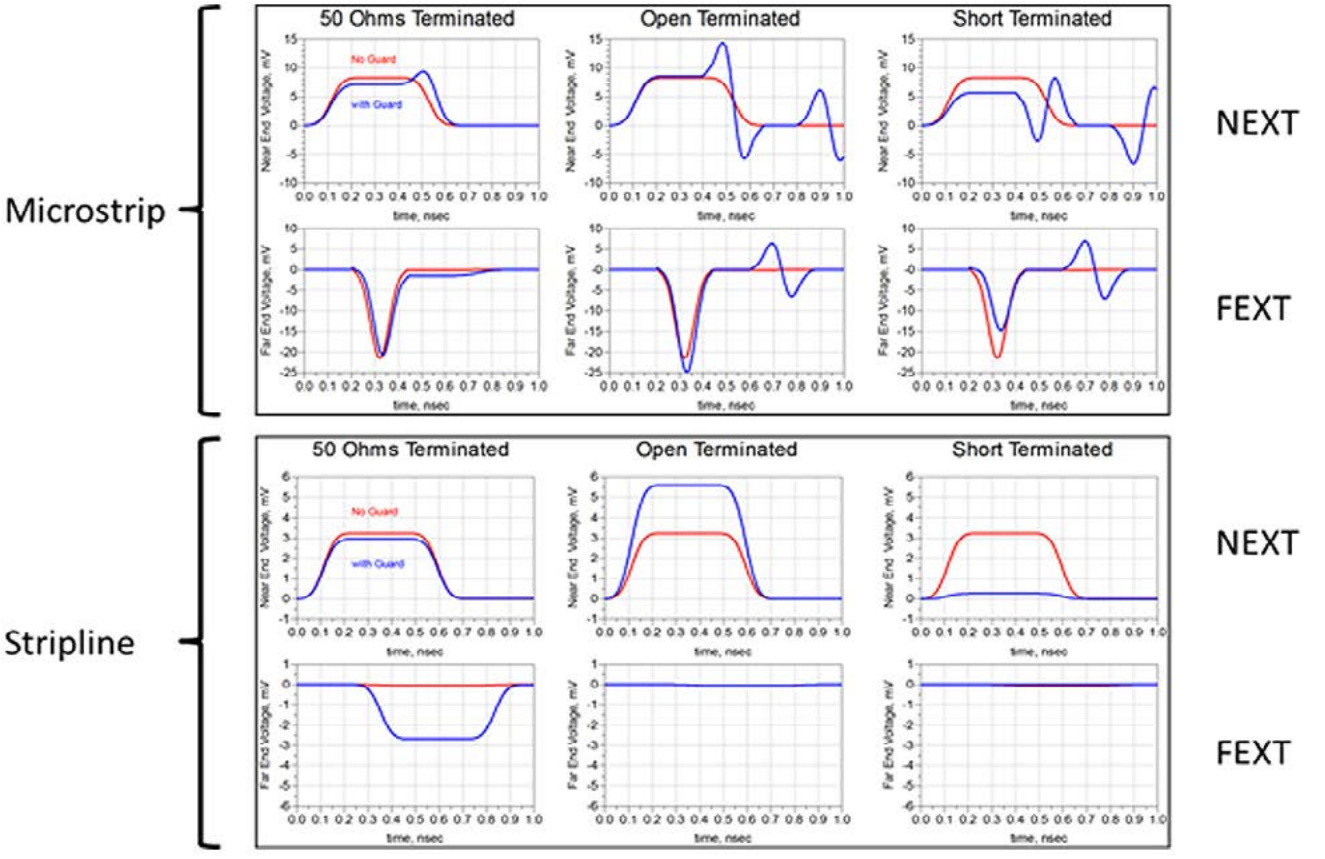

Figure 2: Summary of simulation results when the ends of the guard trace were terminated, left open or shorted to ground for microstrip and stripline geometries.

trace. Because of this, the only real way to analyse the effect is through circuit modeling and simulation.

In microstrip topologies, as you can see, there is little to no benefit to adding a guard trace, regardless of how the ends are terminated. This is because microstrip topologies are inherently prone to far-end crosstalk. Therefore, any far-end noise coupled onto the guard trace will subsequently reinfect the victim with additional far-end noise, as seen by the additional ringing superimposed on the blue waveform.

In stripline topologies, without a guard trace, no far-end crosstalk is generated. But when a guard trace is added, and depending on how the ends are terminated, any near-end coupled noise on the guard trace can reinfect the victim. It is only when the ends are shorted to ground we see such a dramatic reduction of both near- and far-end noise.

Distributed Shorting Vias

When practically implementing a guard trace to act as a shield, a rough rule of thumb suggests the spacing of shorting vias at least 1/10 the wavelength of the highest frequency content of the signal. For a rise time of 100 psec, the stitching via spacing, to meet 1/10, is 0.18 inches, or nine stitching vias over 1.5 inches.

Figure 3 summarizes the results when a guard trace was stitched to ground at multiple wavelengths compared to the case of no guard. As you can see, in the case of microstrip, when the guard trace is shorted with fewer than nine vias, there is still considerable ringing noise on the guard trace which can reinfect the victim line. But in the case of stripline, having two shorting vias at each end, or any number up to nine shorting vias has the same result. This suggests there is no need for multiple shorting vias, other than at the end of the guard trace,

ARE GUARD TRACES WORTH IT? *continues*

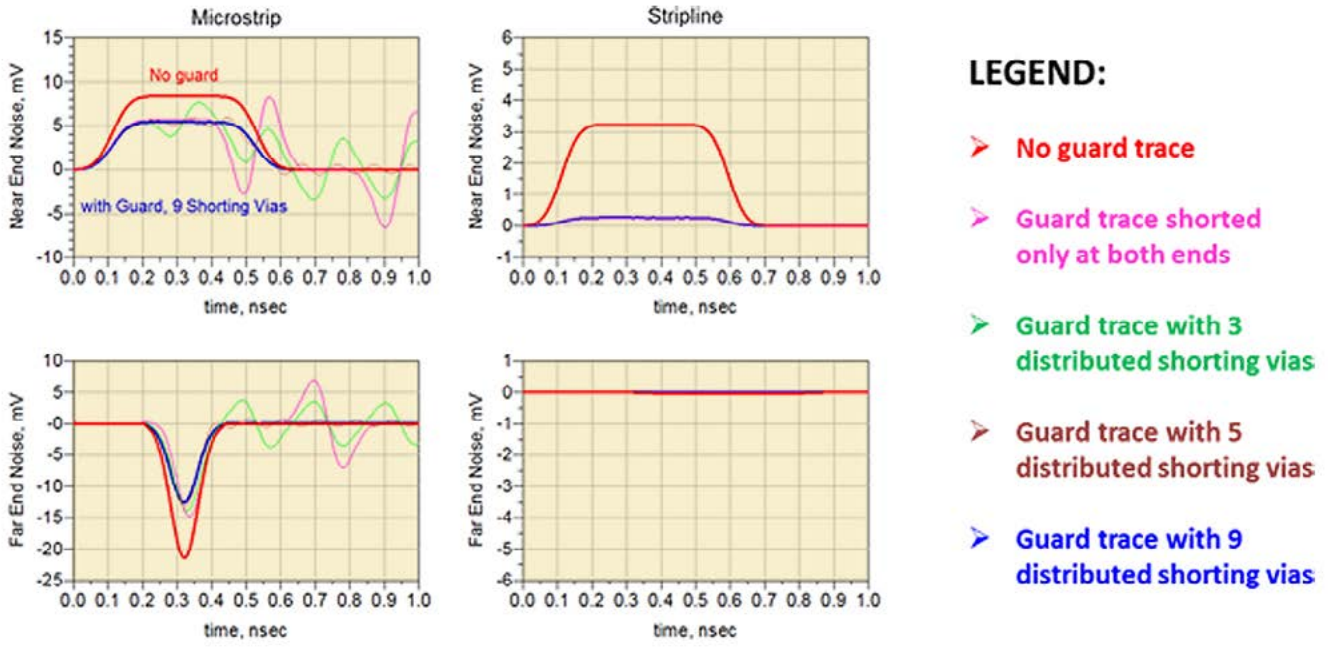

Figure 3: Summary of simulation results with guard trace stitched for microstrip and stripline geometries.

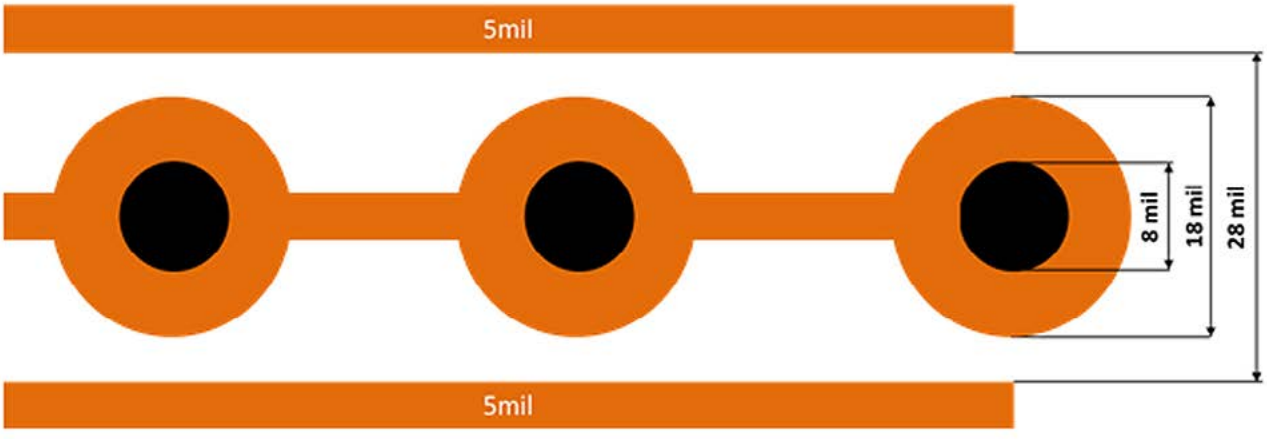

Figure 4: Minimum track-to-track spacing to fit an 8-mil drilled via and pad in through-hole technology.

provided the guard trace is the same length as the coupled length. This dramatically simplifies the use of guard traces in stripline.

Practical Design Considerations

Up to now we have modeled and simulated ideal cases of shorting the guard traces to ground. But in reality, there are additional practical design considerations to consider. First is via size, and the impact it has on the line to line spacing. Next is the finite via inductance, since its impedance will prevent complete suppression of the noise on the guard trace. And finally, the extension of the guard trace compared to the coupled length.

Because through-hole manufacturing design rules limit the smallest via and capture pads, the smallest mechanical drill size most PCB vendors

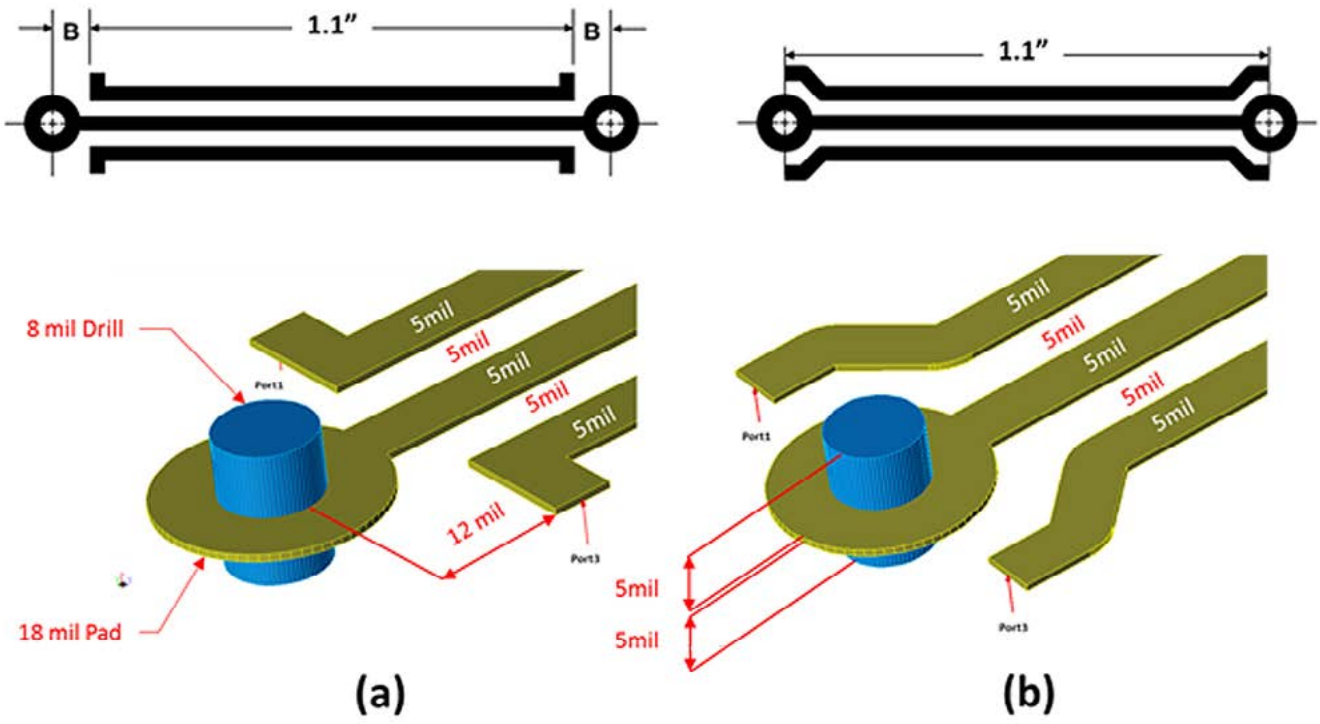

Figure 5: Two examples of adding a grounded guard trace with minimum spacing of 3 x line width. (a): guard trace is extended past the coupled length (A) by dimension B on both sides in order to satisfy minimum 5-mil pad-track spacing requirements. (b): guard trace is equal to coupled length by separating the traces at each ends. Modeled in Agilent Momentum 3D field solver. For clarity, reference planes are not shown.

will spec is 8 mils. By the time you factor in the minimum pad diameter and pad to copper spacing, the minimum space between the aggressor and victim lines would have to be at least 28 mils, as shown in Figure 4, just to fit a guard trace with grounding vias down its length.

At this point, you have to ask yourself if it is even worth it, especially for microstrip topologies. If the two signal lines were to be increased to 28 mils, the reduction in crosstalk from just the added separation would likely be more significant than adding the shorted guard trace.

Fortunately, the circuit analysis has shown there is little benefit to adding a guard trace to microstrip topologies, even if it was ground stitched appropriately. But to gain a dramatic reduction in crosstalk in stripline all that is required is to short the guard trace at each end, and ensure the guard trace is exactly the same length as the coupled length. This means the minimum space to fit a via and guard trace can remain at three times the line width, as long as the guard trace is extended slightly, as shown in Figure 5(a). Alternatively, the guard trace can be made equal to the coupled length, as illustrated in Figure 5(b).

Agilent's ADS Momentum planar 3D field solver was used to explore and quantify the implications vias and guard trace lengths have on noise reinfection. Figure 5 details a portion of the 3D model on the left end of the respective topologies. The right hand sides are identical. The reference planes are not shown for clarity.

After simulation, the S-parameter data was saved in Touchstone format and brought into ADS for transient simulation analysis and comparison. Figure 6 shows the results. The plot on the left used 100 psec rise time for the step edge, while the plot on the right used 50 psec. Both plots are consistent with the dramatic noise reduction observed in Figure 2, except that we see some added noise ripple after about 0.8 nsec.

ARE GUARD TRACES WORTH IT? *continues*

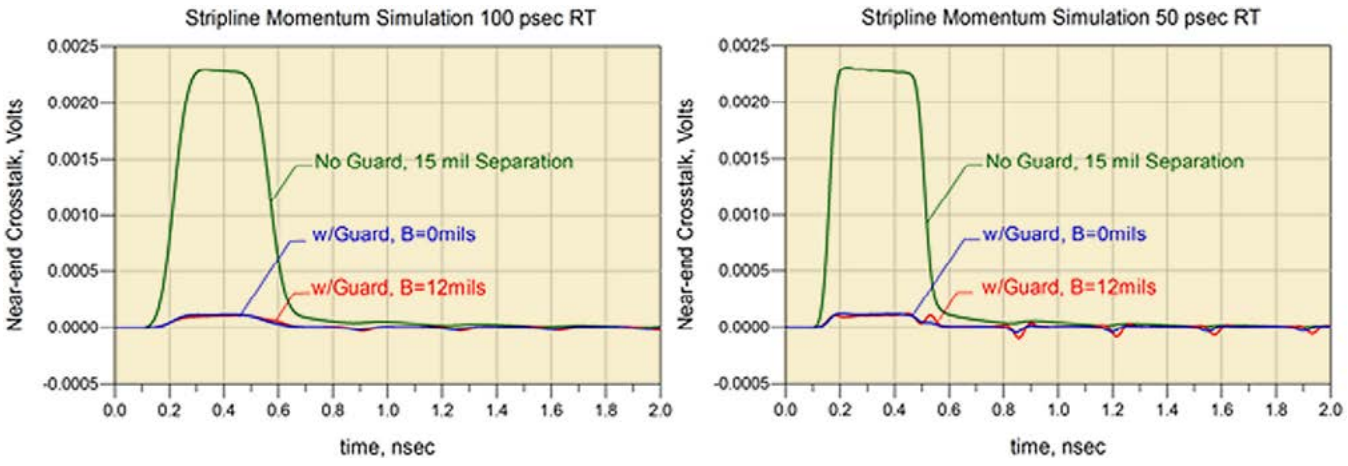

Figure 6: Momentum transient simulation results comparing near-end crosstalk at Port 1 when aggressor voltage was applied to Port 3. The red and blue waveforms are with a guard trace. The green waveform is with no guard and 15 mils separation. Aggressor voltage = 1V, 100 psec rise time (left) and 50 psec rise time (right).

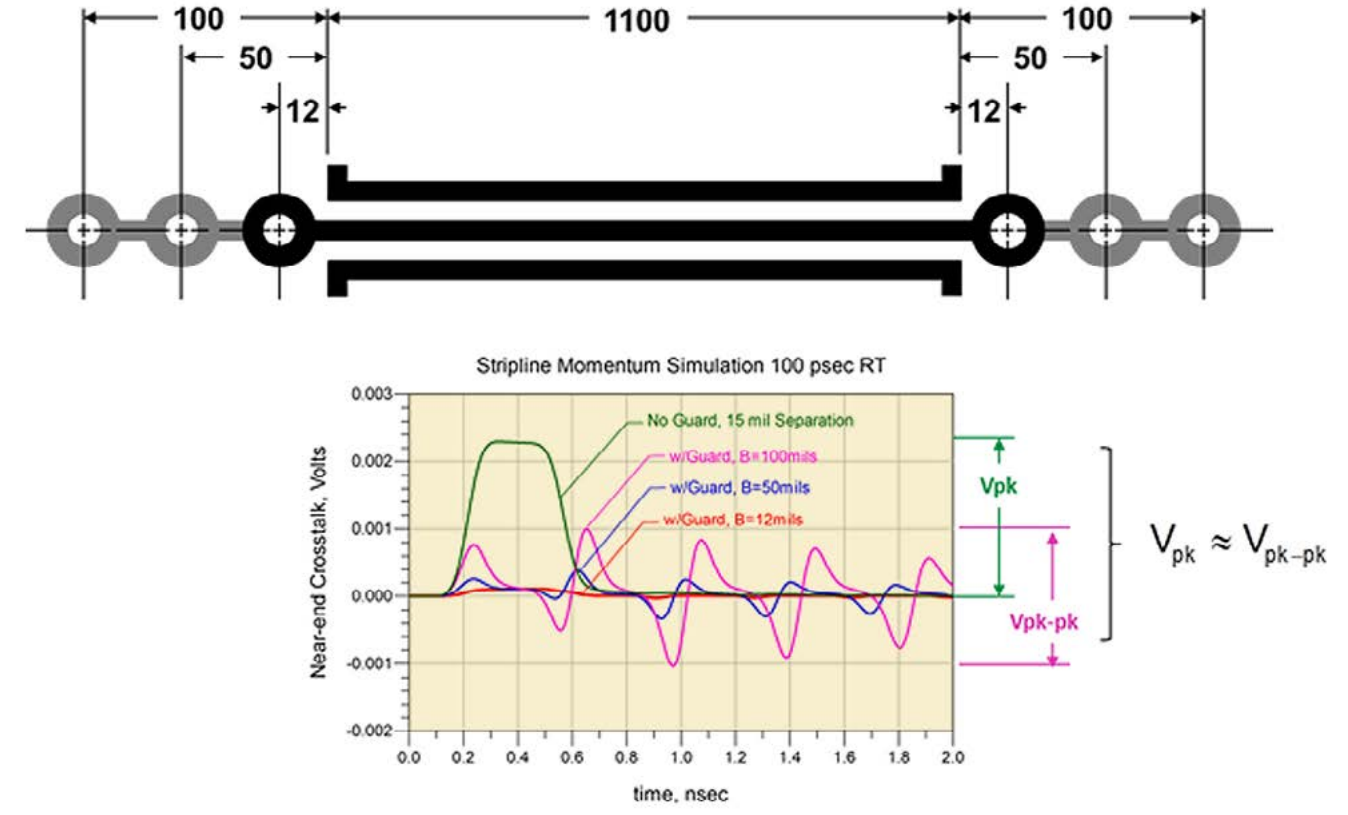

Figure 7: Momentum transient simulation results with guard trace extended. B = 12 mils (red), B = 50 mils (blue) and B = 100 mils (magenta) compared to no guard (green). Aggressor voltage = 1V, 100 psec rise time. Dimensions in mils.

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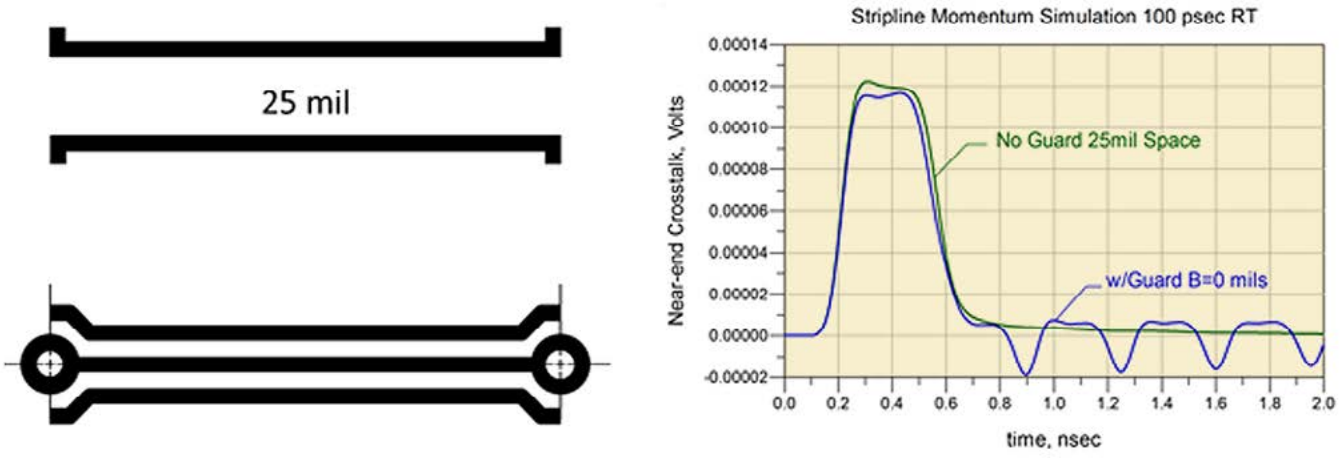

Figure 8: Momentum transient simulation results comparing near-end crosstalk at Port 1 when aggressor voltage was applied to Port 3. Aggressor voltage = 1V, 100 psec rise time.

At 100 psec rise time, there is effectively no difference in near-end noise signature for either (a) or (b) topology. But when the rise time was reduced to 50 psec, the noise ripple is more pronounced. The blue waveform shows that even when dimension B is zero mils, there is still a small amount of noise due to the inductive length of the vias to the reference plane. The red waveform shows that by adding just 12 mils to the guard trace length, at each end, the ripple magnitude is almost doubled.

It is a well-known fact that technology advancements over time results in faster and faster rise times. If you have engineered your design on the technology of the day, any future substitution of parts, with faster rise time, may cause your product to fail, or worse be intermittent.

To explore this phenomenon, the guard trace was varied by 50 and 100 mils at each end, as illustrated in Figure 7. Here we can see that as the guard trace gets longer at each end, the noise ripple grows in magnitude quite rapidly. It is remarkable to note that when the guard trace is just 100 mils longer at each end, the peak-peak amplitude of the noise just about equals the peak magnitude of the no-guard case.

When the guard trace was removed, and the space was increased to five times the line width, the near-end crosstalk was reduced in magnitude and was approximately equal to the guard trace scenario, as seen in Figure 8. Furthermore, because there is no guard trace, there is no additional noise ripple.

So getting back to the original question: Are guard traces worth it? You be the judge. Using a guard trace, shorted at each end, can be effective if you need the isolation. But this approach does have caveats. If you decide to go down this path, it is imperative for you to model and simulate your topology, preferably with a 3D field solver, before signing off on the design. **PCBDESIGN**

Reference

1. Eric Bogatin, Bert Simonovich, "Dramatic Noise Reduction using Guard Traces with Optimized Shorting Vias," DesignCon2013, Santa Clara, CA, USA, Jan 28-31.

Bert Simonovich spent 32 years at Bell Northern Research/Nortel Networks as an electronic engineering technologist. After leaving Nortel in 2009, he founded Lamsim Enterprises Inc., where he provides innovative signal integrity and backplane solutions as a consultant. You can contact Bert through his web site at Lamsimenterprises.com.

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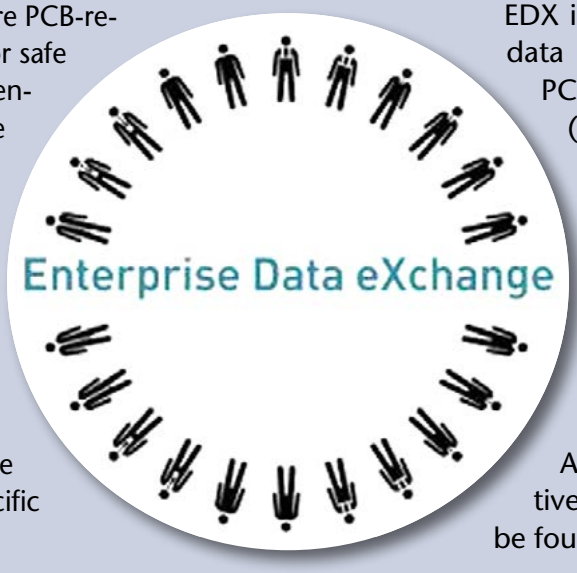
EDX Alliance Ensures PCB Design Data Transfer Security

The Enterprise Data eXchange (or EDX) Solutions Alliance has been established to provide an open industry forum for the broad adoption of its new standard, EDX. EDX is a new and robust data format created to capture PCB-related IP in a standard form for safe and secure data-sharing with enterprise systems and remote third parties. Managing and maintaining data integrity with today's increasing PCB design complexity has become a paramount concern as data is shared with groups requiring access to this IP. The current interfaces to move or share this data are ad-hoc and often tied to specific EDA software versions.



Thus, the EDX format protects the integrity of all product data and the native design data, as well as their relationships. As design tools continue to advance, the EDX structure remains consistent and intact; only content of the native files change but not the interfaces to share the data.

EDX is an XML-in-ZIP format. All data types associated with the PCB design are supported (native design data, library data, related component data, BOMs, manufacturing files, ODB++ as the product model, and viewable files such as PDF and EDIF).

Additional information about the EDX Solutions Alliance and the partners actively adopting the format can be found at www.edx-sa.com.

Electromagnetic Fields: Part 2

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

SUMMARY: In last month's column, Barry Olney discussed how magnetic fields revolve around the earth and how these fields are also present in a multilayer board. Part 2 will look at how electromagnetic fields influence transmission lines and how they can be applied in a BEM field solver.

In last month's column, Electromagnetic Fields: Part 1, we looked at how magnetic fields revolve around the earth and how these fields are also present in a multilayer board. In Part 2, we will look at how electromagnetic fields influence transmission lines and how they can be applied in a BEM field solver.

Maxwell's Equations describe the relationship between electric and magnetic fields. These equations describe the field strength and current density within a closed-loop environment. They require extensive knowledge of higher-order calculus, so I will not bore you (or me) with further details. However, much insight into high-speed design can be gained by understanding the behavior of transmission lines and their associated electromagnetic fields.

In Figure 1, copper is poured around the differential pair. This configuration is commonly used in RF design and called coplanar wave guides. As mentioned in my previous column Ground Pours: To Pour or Not to Pour?, this is not a particularly good strategy for high-speed, digital design as it tends to alter (lower) the impedance of traces that run adjacent to a ground pour area. The traces of the differential pair are still coupled to each other and the ground plane, but are also coupled to the copper pour. This will reduce the impedance by ~25% and provide little additional shielding as the ground plane below is already used as a reference plane.

Figure 2 shows how the fields interact for two common stripline configurations: edge coupled differential (top) and offset, broadside coupled differential (bottom). In the top example, the traces are closely coupled to each other and also to the ground plane above. Since they are located much closer to that plane, the fields follow the path of least inductance rather than coupling to the plane further below (although it does have some influence).

In this case, the ground plane above will be used for the current return path of the signal. It is crucial to understand which plane will be used for the return current path. In general, for offset striplines, whichever plane is closest to the trace has the most influence on impedance.

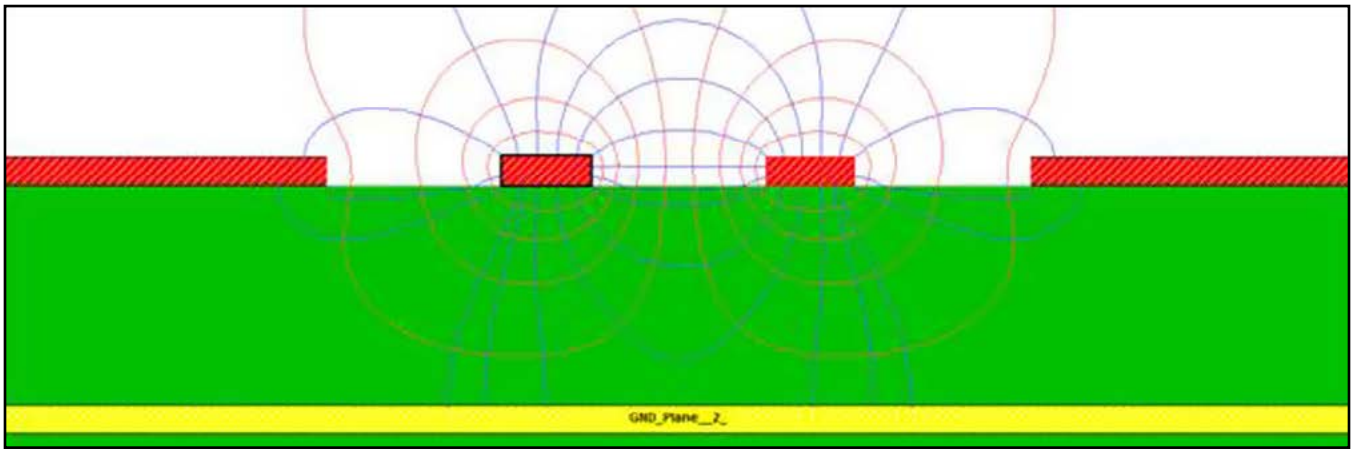


Figure 1: Differential pair as a coplanar wave guide.

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ELECTROMAGNETIC FIELDS: PART 2 *continues*

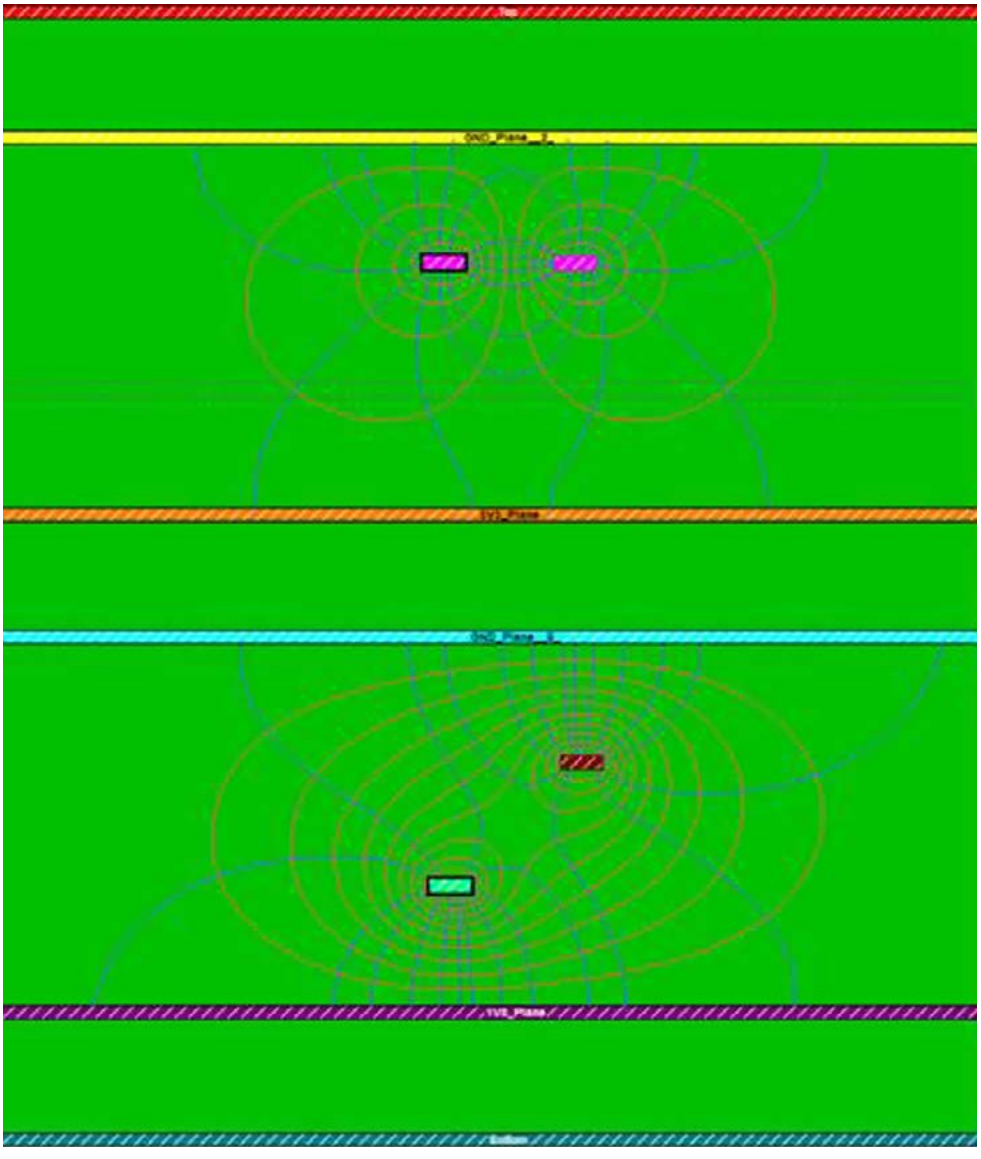

Figure 2: Edge-coupled differential (top) and broadside coupled differential (bottom).

Smack in the middle – both planes are equally important. But this would not be a good layout approach as both would also equally act as the return path. Therefore, a deliberate offset is advised to eliminate this possibility and to be absolutely sure that the correct plane will be used for the return path.

In the bottom example, each trace is coupled to the nearest plane and loosely (offset) broadside coupled to each other. This coupling should be avoided in multilayer boards as it causes crosstalk. It is best to route these two signal layers orthogonally or better still – only have one signal layer between planes to totally eliminate this issue.

The impedance of broadside coupled traces is affected by the mechanical registration of layers of the substrate during the fabrication process. IPC recommends layer-to-layer registration between any two adjacent layers to be within two mils. As you can imagine, the likelihood of two traces aligning perfectly is low. For instance, for a 4-mil trace, it could well be that there is only an overlap of two mils. One possible application where broadside coupling may have an advantage over edge coupled traces, is when routing an interleaved bus on a backplane – routing a number of differential pairs through a succession of connector pin fields where only a single trace fits between pins.

A boundary element method (BEM) field solver, such as that integrated in the ICD Stackup Planner, harnesses the field charges surrounding the traces to calculate an impedance matrix. The boundaries (both dielectric/metal and dielectric/dielectric) are split into many elements and each element is assumed to have a uniform charge density. Hence, small elements are needed where the charge density changes rapidly and larger elements where the charge density is more uniform. Defining the elements is as much an art as a science and this all impacts on the speed of simulation. Green's Theorem Method and the matrix inversion yield a solution of an integral equation.

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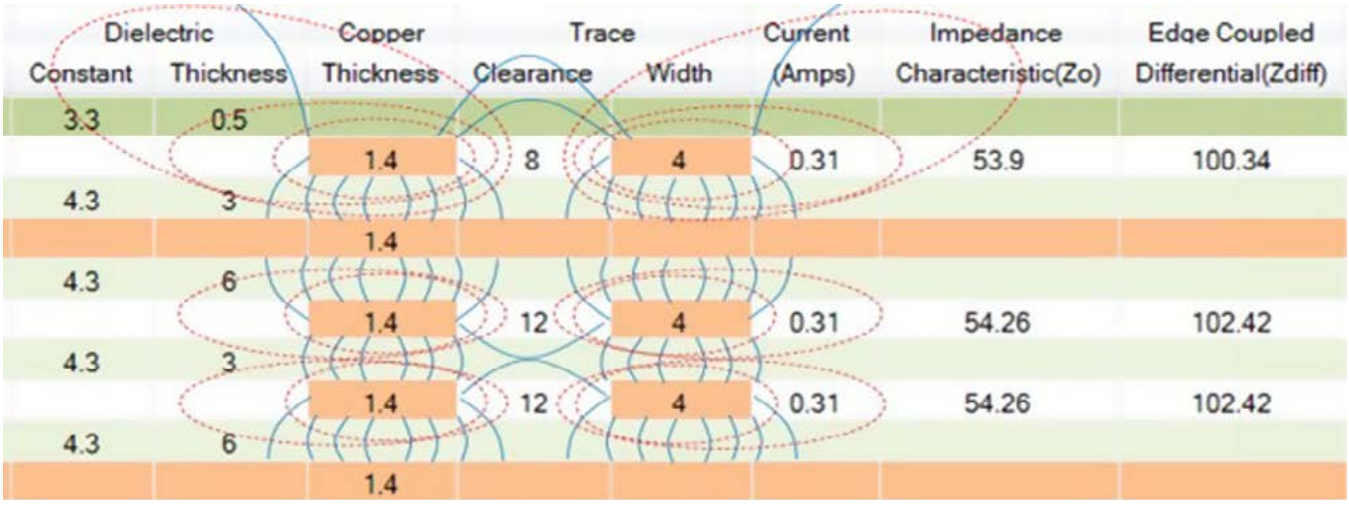
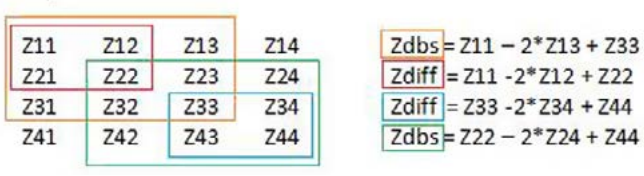


Figure 3: The electromagnetic fields as seen by the field solver in the ICD Stackup Planner.

To increase simulation speed, ICD has developed unique, proprietary algorithms to automatically adjust the solution space relative to the defined variables.

In Figure 3, I have roughly drawn in the fields that would be seen by the field solver software. A 16-element impedance matrix is required to extract all the values of the stripline configuration (layer 3 & 4) where there are two signal layers between the planes.

Equation 1



where Zdiff is edge coupled and Zdbs is broadside coupled differential impedance

The impedance matrix gives the impedance of the system of coupled nets in the coupling region. The values in the diagonal matrix positions (example Z12 and Z21) can be thought of as giving the impedances to ground of the corresponding nets, accounting for the presence of the other nearby, coupled traces. When an IC drives into one of the lines, however, it "sees" not only the diagonal impedance for that line, but also some of the off-diagonal terms in the matrix.

For traces that are only weakly coupled, the diagonal impedance terms are dominant, and the diagonal values are close to what they would be if the lines were completely isolated from each other. As the coupling becomes stronger, the diagonal terms deviate more from their standalone values, and the off-diagonal terms increase.

If the configuration is microstrip or embedded microstrip (rather than stripline), and the electromagnetic fields they generate lie in a mixture of dielectrics (e.g., FR-4 and air), then multiple propagation velocities exist per line.

Much insight into high-speed design can be gained by understanding the behaviour of transmission lines and the influence of their associated electromagnetic fields. Controlled impedance design can be simplified and the path of the return current can be visualized by understanding the field coupling.

Points to remember:

- Maxwell's Equations describe the relationship between electric and magnetic fields. Green's Theorem method and the matrix inversion yield a solution of an integral equation.
- Return current paths follow the path of least inductance rather than coupling to a plane further away.
- For offset striplines, whichever plane is closest to the trace has the most influence on

impedance. A deliberate offset is advised to eliminate this possibility and to be absolutely sure which plane will be used for the return path.

• The impedance of broadside coupled traces is affected by the mechanical registration of layers, of the substrate, during the fabrication process and should be avoided.

• A BEM field solver, such as that integrated in the ICD Stackup Planner, harnesses the field charges surrounding the traces to calculate an impedance matrix.

• The impedance matrix gives the impedance of the system of coupled nets in the coupling region. **PCBDESIGN**

References

1. Advanced Design for SMT Course – Barry Olney

2. Beyond Design: Embedded Signal Routing – Barry Olney

3. Beyond Design: Ground Pours: To Pour or Not to Pour? – Barry Olney

4. Beyond Design: Controlling the Beast – Barry Olney

5. Digital Transmission Lines – Ken Granzow

6. EMC and the PCB – Mark Montrose

7. The ICD Stackup and PDN Planner can be downloaded from www.icd.com.au

8. All trademarks are registered by their respective owners.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company is a PCB design service bureau that specializes in board-level simulation, and is the developer of the ICD Stackup Planner and ICD PDN Planner software. Contact Barry here.

EDX: A New Standard for Sharing PCB IP

by Jody Miller
MENTOR GRAPHICS CORPORATION

SUMMARY: The integration of PCB design flow data with enterprise and third-party systems is often a one-off task for each environment. The new single-file format Enterprise Data eXchange can help streamline this task.

Over time, the challenges in electronic product design have changed, just as significantly as the electronics themselves. The challenges designers faced when printed circuit boards had one or two sides and a handful of 16-pin ICs were completely different than today's challenges with multilayer, high-speed PCBs running 1,000 times faster. In a recent study conducted by The Aberdeen Group, it was found that the top three challenges for electronics companies in managing PCB design data were:

1. Integrating PCB data with enterprise systems
2. Complexity of the PCB data
3. Exchanging PCB data with external sites and third-party providers

The increase in data complexity has been fueled by major advancements in moving to concurrent, collaborative design flows. This has im-

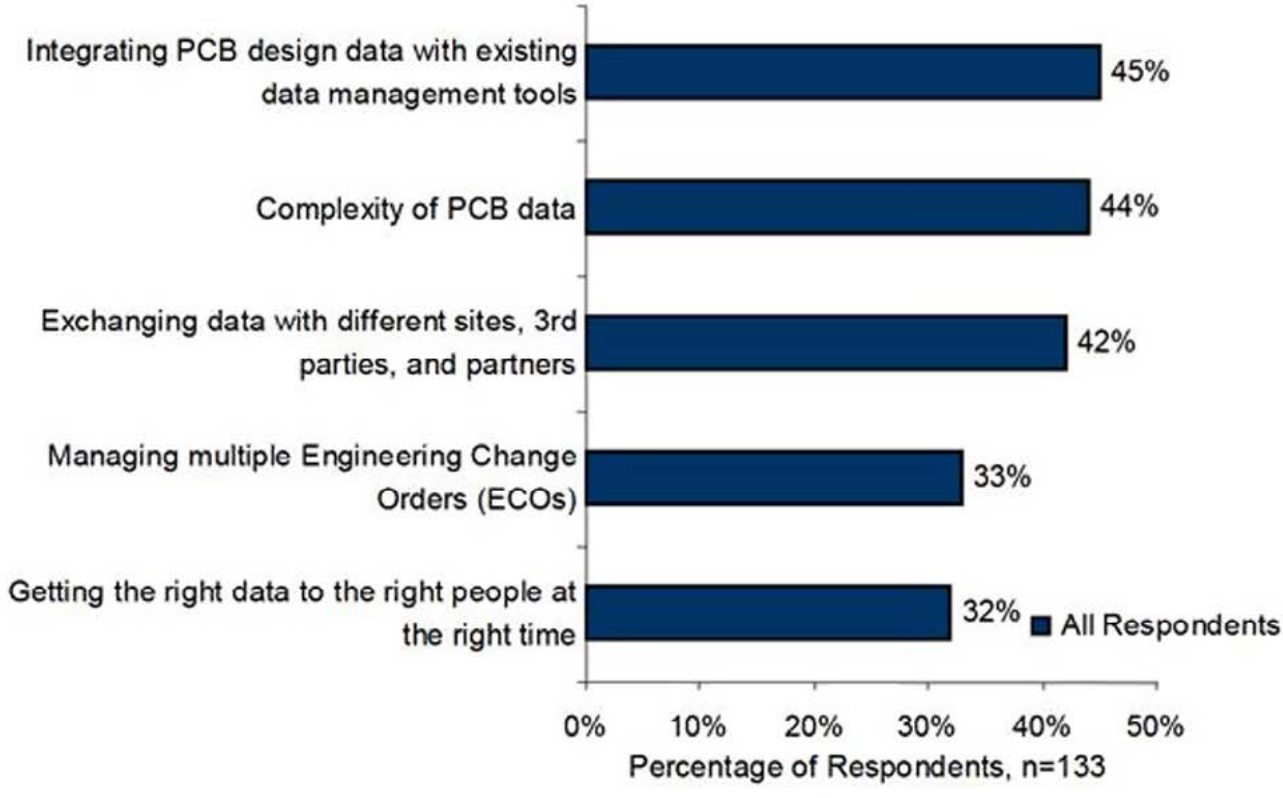


Figure 1: The top challenges facing electronics companies. (Courtesy of The Aberdeen Group)

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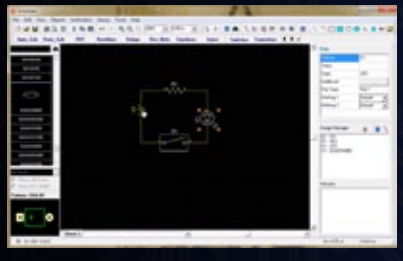
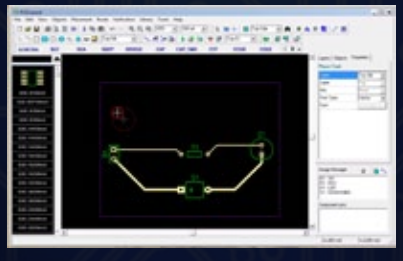
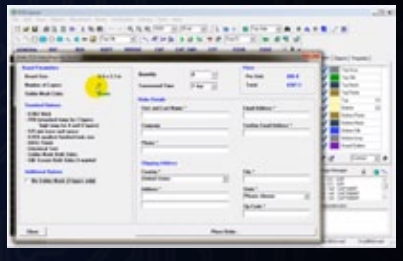


2 CONVERT TO PCB



3 ORDER YOUR BOARDS



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pacted how data structures have been defined within a design environment. Understanding these relationships and managing the individual design and library objects often require extensive domain knowledge of all data objects created or modified by any tool in the design process. Protecting the data and these relationships is critical to enabling reuse of the data.

Commonly, the integration of this data to PLM, ERP, or CIS systems becomes a one-off task for each environment, which is often tied to specific interfaces, tool versions, and/or data structures. Companies need the flexibility to upgrade their PCB design flow independently of existing interfaces to tools and infrastructure surrounding the design process. Typical examples are the introduction of new routing technologies, design to manufacturing tools and checks, or work-in-process management within the PCB design flow. Interfaces from the design flow to any third-party tool or enterprise system must be implemented without any dependency on proprietary file formats or objects.

Also, exchanging complete data sets with remote sites, contract manufacturers, or service bureaus can be a challenge. Ensuring they have the complete data set, and that it can be easily restored in their environment is necessary to enable congruous design or manufacturing activities without stoppage.

These requirements were compelling reasons that drove the definition of a new data exchange format called Enterprise Data eXchange or EDX. This new format allows integration of the PCB design flows with other enterprise systems or third parties, in a reliable release-independent manner.

The Need for a New Standard

In evaluating data formats to help solve the challenges described above, it became clear very quickly that existing standards did not meet all of the needs. Multiple formats and data standards, such as PDX, ECIX, and VSIA were evaluated before defining EDX as a new standard. The findings were that none of these supported all of the requirements necessary to enable transfer of active, in-process design data. Some of the specific factors considered included:

- Data security in protecting the native data sets: Current standards do not enable protection of core relationships of specific data subsets. If the standard did include security considerations, it was at a very general level.
- Data flexibility and the ability to represent a multitude of data types: Some of these standards were focused only on SoC data sets – not PCB data sets. Other standards did not allow for extensions to support the full range of PCB data requirements (i.e., design files, BOMs, test plans, functional specifications, FPGA program files, etc.).
- The ability to represent work actions to support active workflows: The standards evaluated did not include support for bi-directional work instructions to support PCB-specific workflows.

How it Works

EDX is a single-file format definition designed to facilitate sharing PCB design data between the engineering groups and the extended enterprise. EDX uses a combination of an Open Packaging Convention container to hold the data files, a system of manifest files to organize the content and the latest digital signature technology to provide a secure and reliable data exchange and archive. EDX is flexible in that it supports all the data types associated with PCB design, and is flexible enough to incorporate additional data objects that users may want to associate with the design, i.e., functional specs, test results, spec control drawings for library parts, etc.

To protect against unauthorized modification of the PCB data, the content of an EDX package is signed using digital signatures at two levels: on the overall package and at the container level. This enables the recipient to verify that the package of data has not been tampered with after it was created and the design flow to make sure that the integrity of the design databases has been preserved. In an EDX world, design and library objects can only be stored as a complete container outside the authoring environment, avoiding unauthorized manipulation. Proprietary data structures and their associated objects cannot be safely modified outside of the au-

thoring environment if data integrity is to be protected.

The EDX format integrates design processes and the enterprise systems without the need to access detailed design objects. EDX provides the vehicle to include established standard output formats along with the design databases. PDF, EDIF and ODB++ are just some of the formats that may be used within EDX to provide a view of the design intent without the need to access the native design files. By representing the data in a consistent EDX format, independent of any of the tools creating it or reading it, interfaces can be established which are version-independent. As the design tools continue to advance, the EDX structure remains consistent. It is only the details within the native files themselves change – not the interfaces sharing the data.

Integration with Third-Party Systems

EDX provides a single package that includes not only the native design and library data but also all of the derived outputs that are required by downstream processes.

• EDX has explicit data structures to support the PCB design and library data together with the derived files. This makes it much easier to differentiate between the design data bases that should not be modified and the viewable files or manufacturing outputs that can be consumed by the rest of the enterprise.

• EDX utilizes the latest XML security tools to sign the manifests and data files. This enables the recipient to verify that the data has not been corrupted or tampered with since the EDX package was created. This includes the support for either self-signed certificates or using signing certificates that have been obtained from a signature authority. These security measures enable the PCB tool vendor to verify the state of their design data databases before importing them into their tools.

These features also make EDX a good choice for handing data off to contract manufacturers or design partners. Placing all of the data required in a single package and signing it secures against the risk of sending incomplete or inconsistent instructions to the manufacturer.

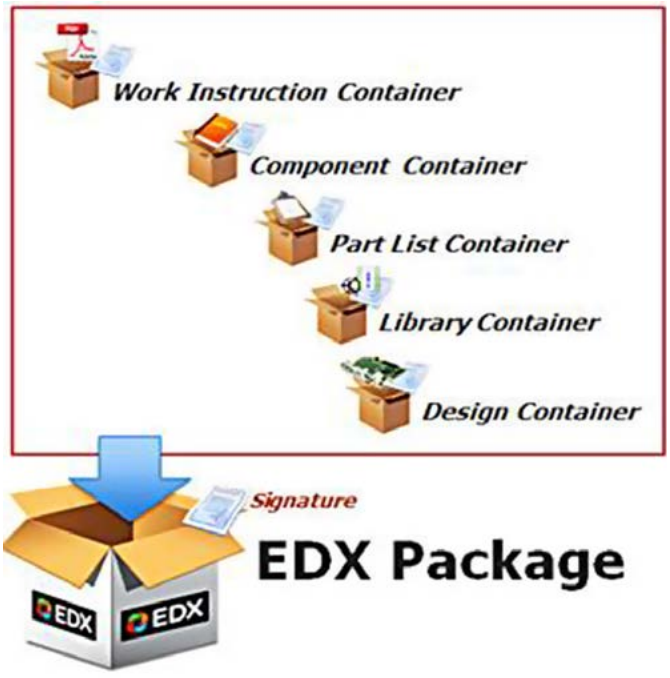

Figure 2: The EDX package manifest includes containers for work instructions, component data, parts list, library, and design data.

Process Integration Support

EDX not only enables exchange of library and design data, but it also integrates PCB-related processes via work instructions. In two common applications of the work instruction package, it's possible to send a new part request that was raised in a third-party system to the librarian or initiate an engineering change order to the design lead.

Because EDX is based on the Open Packaging Convention, it is possible to include the datasheet for the new part or a set of marked up drawings for the design change. This makes it easy to accurately communicate the requirements or markups to the engineering team. The manifest layer enables status information to be communicated between the engineering department and the rest of the enterprise. Enterprise users can view the current status of the part request or the ECO of interest.

EDX facilitates sharing PCB IP across the enterprise, protects the shared data throughout its life cycle, ensures that remote sites and third parties can receive data with confidence, and that data complexities can be managed to protect integrity of native data.

In addition:

1. EDX is a stable robust interface standard for exchanging data between the PCB design flow and the enterprise infrastructure or other third-party solutions.
2. EDX is independent of the version and data formats of the authoring tools used to read/write it, allowing the design tools to evolve without impacting data exchange with third party solutions.
3. Integration built using EDX does not need to be reworked with every release of a PCB design flow.
4. EDX utilizes industry standard neutral files like PDF, EDIF and ODB++ for viewable objects.
5. EDX provides a single file for exchange with the authoring environment; all design data can be exported via a single EDX package.
6. The EDX format makes extensive use of XML digital signatures to ensure that the content of the file has not been changed since it was generated. This is very useful when using EDX to send data to a contract manufacturer for manufacturing or review. If the signatures are still valid, the manufacturer can be sure that the data set received is consistent.
7. EDX is based on standards such as OPC and IPC-2581. This ultimately reduces your risk in embracing the standard as these provide a proven base to build on.

The EDX Solutions Alliance is open to designers, solution providers, and anyone interested in enabling adoption of the standard. **PCBDESIGN**

Jody Miller has over 20 years of experience in the PCB industry, including extensive work with EDA and component information/data management systems providers. She is currently working in the Board Systems Division for Mentor Graphics.

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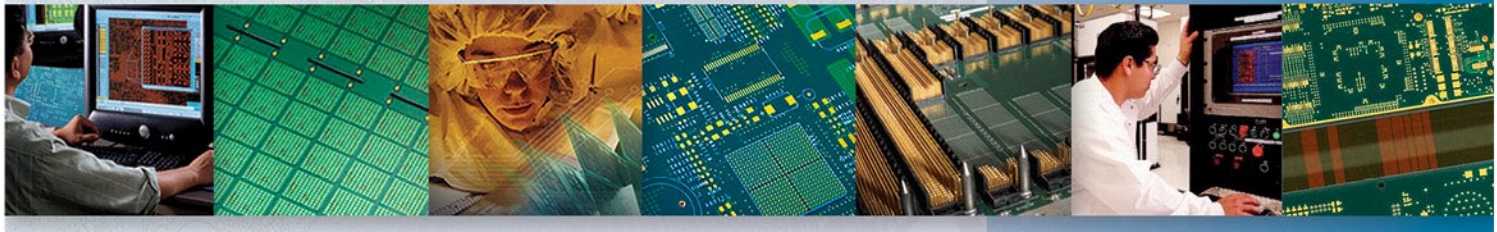

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TOP TEN

Most-Read News Highlights from PCBDesign007 this Month

① Letters: Few New PCB Designers, And No Wonder

"I have noticed the lack of younger designers since the early 1990s," writes Joe Bates. "This is indeed a disturbing trend. Even more unsettling, though, is the increasing trend of companies looking for PCB designers who are experienced in multiple CAD tools, with EE degrees and mechanical design experience. All of this for $35,000 to $45,000 a year."

② Mentor FloTHERM XT Combines EDA, Mechanical Design

This cooling simulation tool enables earlier virtual prototyping, fewer design iterations, and advanced "what-if" analysis. Design teams in the automotive, aerospace, telecommunications, computing, industrial automation, and consumer electronics markets can benefit from FloTHERM XT.

③ EMA Introduces Team Design Capability for OrCAD

"Our engineers saw first-hand the challenges design teams were facing when trying to work collaboratively on schematic projects using traditional methods like shared drives and email threads. We decided there had to be a better way," said Manny Marcano, president and CEO of EMA.

④ Letter: IPC-2581 is the Open, Neutral, Global Standard

"I was disappointed that you didn't mention (or you didn't know) that IPC-2581 is the open, neutral, globally supported standard for design data transfer that is being promoted by PCB design and supply chain companies," writes Hemant Shah of Cadence Design Systems.

5 ICD Releases Stackup Planner for Altium Designer 2013

In-Circuit Design Pty Ltd (ICD), Australia, in conjunction with Desktop EDA Pty Ltd, have released a new Stackup Planner for Altium Designer 2013. The bi-directional interface imports the substrate configuration from the ICD Stackup Planner and automatically creates the corresponding layers in Altium Designer configuring the Layer Stackup Manager.

6 EDA Consortium Ends 2012 with Record Revenue in Q4

"The EDA industry finished 2012 with a record quarter," said Walden C. Rhines, board sponsor for the EDAC MSS and chairman and CEO of Mentor Graphics. "CAE, IP and PCB were all strong, with PCB at 19.5% growth, more than double that of any other major category. Geographically, all of the regions reported positive growth, with the Europe/Middle East/Africa region leading the way."

7 Agilent Launches Recognition Program for EDA Experts

Agilent Technologies has launched the Agilent Certified Expert recognition program for electronic design automation experts. Eligible participants include individuals demonstrating a high level of expertise, both theoretical and practical, in applying Agilent EEsof EDA tools for product design and modeling.

8 Cadence to Acquire Tensilica for $380 Million

Tensilica provides configurable dataplane processing units that are optimized for embedded data and signal processing targeted at mobile wireless, network infrastructure, auto infotainment and home applications. The company had approximately $30 million in cash at the end of 2012.

9 EDX Alliance Ensures PCB Design Data Transfer Security

The Enterprise Data eXchange (EDX) Solutions Alliance was established today to provide an open industry forum for the broad adoption of its new standard, EDX. EDX is a new and robust data format created to capture PCB-related IP in a standard form for safe and secure data-sharing with enterprise systems and remote third parties.

10 IEEE Launches Study Group to Explore 400 Gb/s Ethernet

IEEE has launched the IEEE 802.3™ "Standard for Ethernet" study group to explore development of a 400 Gb/s Ethernet standard to efficiently support ever-increasing, exponential network bandwidth growth. The IEEE 802.3 Ethernet Bandwidth Assessment report forecast that networks will need to support 58% CAGRs on average.

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April 16-18, 2013
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Application of Printed, Organic & Flexible Electronics
April 17-18, 2013
Berlin, Germany

DESIGN West
April 22-25, 2013
San Jose, California, USA

Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT 2013)
April 23-25, 2013
Orlando, Florida, USA

NEPCON China 2013
April 23-25, 2013
Shanghai, China

2013 Defense, Security, and Sensing Exhibition
April 29 - May 3, 2013
Baltimore, Maryland, USA

2013 AASRI Conference on Parallel and Distributed Computing and Systems
May 1-2, 2013
Singapore

EDS
May 6-9, 2013
Las Vegas, Nevada, USA

13th Electronic Circuits World Convention
May 7-9, 2013
Nuremberg, Germany

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Next Month in *The PCB Design Magazine*

Board densities continue to increase, and blind and buried vias are popping up on PCBs of all kinds. How does this ever-advancing HDI technology affect the job of the PCB designer? Our contributors lay out the best ways to "get small."

See you in May!